



Section I. Stratix II GX Device Data Sheet

This section provides designers with the data sheet specifications for Stratix® II GX devices. They contain feature definitions of the transceivers, internal architecture, configuration, and JTAG boundary-scan testing information, DC operating conditions, AC timing parameters, a reference to power consumption, and ordering information for Stratix II GX devices.

This section includes the following chapters:

- [Chapter 1, Introduction](#)
- [Chapter 2, Stratix II GX Architecture](#)
- [Chapter 3, Configuration & Testing](#)
- [Chapter 4, DC and Switching Characteristics](#)
- [Chapter 5, Reference and Ordering Information](#)

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

The Stratix® II GX family of devices is Altera's third generation of FPGAs to combine high-speed serial transceivers with a scalable, high-performance logic array. Stratix II GX devices include 4 to 20 high-speed transceiver channels, each incorporating clock and data recovery unit (CRU) technology and embedded SERDES capability at data rates of up to 6.375 gigabits per second (Gbps). The transceivers are grouped into four-channel transceiver blocks and are designed for low power consumption and small die size. The Stratix II GX FPGA technology is built upon the Stratix II architecture and offers a 1.2-V logic array with unmatched performance, flexibility, and time-to-market capabilities. This scalable, high-performance architecture makes Stratix II GX devices ideal for high-speed backplane interface, chip-to-chip, and communications protocol-bridging applications.

Features

This section lists the Stratix II GX device features.

- Main device features:
 - TriMatrix memory consisting of three RAM block sizes to implement true dual-port memory and first-in first-out (FIFO) buffers with performance up to 550 MHz
 - Up to 16 global clock networks with up to 32 regional clock networks per device region
 - High-speed DSP blocks provide dedicated implementation of multipliers (at up to 450 MHz), multiply-accumulate functions, and finite impulse response (FIR) filters
 - Up to four enhanced PLLs per device provide spread spectrum, programmable bandwidth, clock switch-over, real-time PLL reconfiguration, and advanced multiplication and phase shifting
 - Support for numerous single-ended and differential I/O standards
 - High-speed source-synchronous differential I/O support on up to 71 channels
 - Support for source-synchronous bus standards, including SPI-4 Phase 2 (POS-PHY Level 4), SFI-4.1, XSBI, UTOPIA IV, NPSI, and CSIX-L1
 - Support for high-speed external memory, including quad data rate (QDR and QDRII) SRAM, double data rate (DDR and DDR2) SDRAM, and single data rate (SDR) SDRAM

- Support for multiple intellectual property megafunctions from Altera® MegaCore® functions and Altera Megafunction Partners Program (AMPPSM) megafunctions
- Support for design security using configuration bitstream encryption
- Support for remote configuration updates
- Transceiver block features:
 - High-speed serial transceiver channels with clock data recovery (CDR) provide 600-megabits per second (Mbps) to 6.375-Gbps full-duplex transceiver operation per channel
 - Devices available with 4, 8, 12, 16, or 20 high-speed serial transceiver channels providing up to 255 Gbps of serial bandwidth (full duplex)
 - Dynamically programmable voltage output differential (V_{OD}) and pre-emphasis settings for improved signal integrity
 - Support for CDR-based serial protocols, including PCI Express, Gigabit Ethernet, SDI, Altera's SerialLite II, XAUI, CEI-6G, CPRI, Serial RapidIO, SONET/SDH
 - Dynamic reconfiguration of transceiver channels to switch between multiple protocols and data rates
 - Individual transmitter and receiver channel power-down capability for reduced power consumption during non-operation
 - Adaptive equalization (AEQ) capability at the receiver to compensate for changing link characteristics
 - Selectable on-chip termination resistors (100, 120, or 150 Ω) for improved signal integrity on a variety of transmission media
 - Programmable transceiver-to-FPGA interface with support for 8-, 10-, 16-, 20-, 32-, and 40-bit wide data transfer
 - 1.2- and 1.5-V pseudo current mode logic (PCML) for 600 Mbps to 6.375 Gbps (AC coupling)
 - Receiver indicator for loss of signal (available only in PIPE mode)
 - Built-in self test (BIST)
 - Hot socketing for hot plug-in or hot swap and power sequencing support without the use of external devices
 - Rate matcher, byte-reordering, bit-reordering, pattern detector, and word aligner support programmable patterns
 - Dedicated circuitry that is compliant with PIPE, XAUI, and GIGE
 - Built-in byte ordering so that a frame or packet always starts in a known byte lane
 - Transmitters with two PLL inputs for each transceiver block with independent clock dividers to provide varying clock rates on each of its transmitters

- 8B/10B encoder and decoder perform 8-bit to 10-bit encoding and 10-bit to 8-bit decoding
- Phase compensation FIFO buffer performs clock domain translation between the transceiver block and the logic array
- Receiver FIFO resynchronizes the received data with the local reference clock
- Channel aligner compliant with XAUI



Certain transceiver blocks can be bypassed. Refer to the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook* for more details.

Table 1–1 lists the Stratix II GX device features.

| Feature | EP2SGX30C/D | | EP2SGX60C/D/E | | | EP2SGX90E/F | | EP2SGX130/G |
|---|------------------------|---|------------------------|-----|-----|------------------------|-----|------------------------|
| | C | D | C | D | E | E | F | G |
| ALMs | 13,552 | | 24,176 | | | 36,384 | | 53,016 |
| Equivalent LEs | 33,880 | | 60,440 | | | 90,960 | | 132,540 |
| Transceiver channels | 4 | 8 | 4 | 8 | 12 | 12 | 16 | 20 |
| Transceiver data rate | 600 Mbps to 6.375 Gbps | | 600 Mbps to 6.375 Gbps | | | 600 Mbps to 6.375 Gbps | | 600 Mbps to 6.375 Gbps |
| Source-synchronous receive channels (1) | 31 | | 31 | 31 | 42 | 47 | 59 | 73 |
| Source-synchronous transmit channels | 29 | | 29 | 29 | 42 | 45 | 59 | 71 |
| M512 RAM blocks (32 × 18 bits) | 202 | | 329 | | | 488 | | 699 |
| M4K RAM blocks (128 × 36 bits) | 144 | | 255 | | | 408 | | 609 |
| M-RAM blocks (4K × 144 bits) | 1 | | 2 | | | 4 | | 6 |
| Total RAM bits | 1,369,728 | | 2,544,192 | | | 4,520,448 | | 6,747,840 |
| Embedded multipliers (18 × 18) | 64 | | 144 | | | 192 | | 252 |
| DSP blocks | 16 | | 36 | | | 48 | | 63 |
| PLLs | 4 | | 4 | 4 | 8 | 8 | | 8 |
| Maximum user I/O pins | 361 | | 364 | 364 | 534 | 558 | 650 | 734 |

Table 1–1. Stratix II GX Device Features (Part 2 of 2)

| Feature | EP2SGX30C/D | | EP2SGX60C/D/E | | | EP2SGX90E/F | | EP2SGX130/G |
|---------|-------------------------|---|-------------------------|---|------------------------------|------------------------------|------------------------------|---------------------------|
| | C | D | C | D | E | E | F | G |
| Package | 780-pin FineLine BGA | | 780-pin FineLine BGA | | 1,152-pin FineLine BGA | 1,152-pin FineLine BGA | 1,508-pin FineLine BGA | 1,508-pin FineLine BGA |

Note to Table 1–1:

- (1) Includes two sets of dual-purpose differential pins that can be used as two additional channels for the differential receiver or differential clock inputs.

Stratix II GX devices are available in space-saving FineLine BGA packages (refer to Table 1–2). All Stratix II GX devices support vertical migration within the same package. Vertical migration means that you can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities. For I/O pin migration across densities, you must cross-reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins are migratable. Table 1–3 lists the Stratix II GX device package sizes.

Table 1–2. Stratix II GX Package Options (Pin Counts and Transceiver Channels)

| Device | Transceiver Channels | Source-Synchronous Channels | | Maximum User I/O Pin Count | | |
|------------|----------------------|-----------------------------|----------|------------------------------------|--------------------------------------|--------------------------------------|
| | | Receive (1) | Transmit | 780-Pin FineLine BGA (29 mm) | 1,152-Pin FineLine BGA (35 mm) | 1,508-Pin FineLine BGA (40 mm) |
| EP2SGX30C | 4 | 31 | 29 | 361 | — | — |
| EP2SGX60C | 4 | 31 | 29 | 364 | — | — |
| EP2SGX30D | 8 | 31 | 29 | 361 | — | — |
| EP2SGX60D | 8 | 31 | 29 | 364 | — | — |
| EP2SGX60E | 12 | 42 | 42 | — | 534 | — |
| EP2SGX90E | 12 | 47 | 45 | — | 558 | — |
| EP2SGX90F | 16 | 59 | 59 | — | — | 650 |
| EP2SGX130G | 20 | 73 | 71 | — | — | 734 |

Note to Table 1–2:

- (1) Includes two differential clock inputs that can also be used as two additional channels for the differential receiver.

Table 1–3. Stratix II GX FineLine BGA Package Sizes

| Dimension | 780 Pins | 1,152 Pins | 1,508 Pins |
|-------------------------|----------|------------|------------|
| Pitch (mm) | 1.00 | 1.00 | 1.00 |
| Area (mm ²) | 841 | 1,225 | 1,600 |
| Length width (mm × mm) | 29 × 29 | 35 × 35 | 40 × 40 |

Referenced Document

This chapter references the following document:

- *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*

Document Revision History

Table 1–4 shows the revision history for this chapter.

Table 1–4. Document Revision History

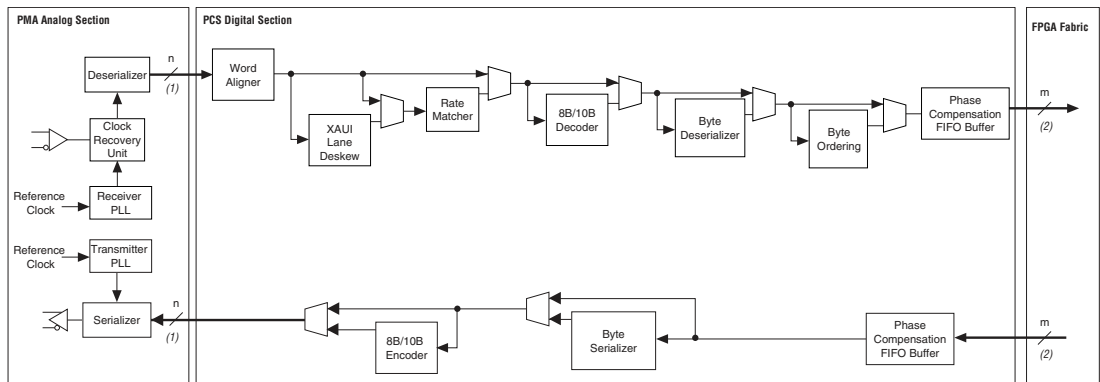
| Date and Document Version | Changes Made | Summary of Changes |
|---------------------------|--|---|
| October 2007, v1.6 | Updated “Features” section. | |
| | Minor text edits. | |
| August 2007, v1.5 | Added “Referenced Documents” section. | |
| | Minor text edits. | |
| February 2007, v1.4 | <ul style="list-style-type: none"> • Changed 622 Mbps to 600 Mbps on page 1-2 and Table 1–1. • Deleted “DC coupling” from the Transceiver Block Features list. • Changed 4 to 6 in the PLLs row (columns 3 and 4) of Table 1–1. | |
| | Added the “Document Revision History” section to this chapter. | Added support information for the Stratix II GX device. |
| June 2006, v1.3 | <ul style="list-style-type: none"> • Updated Table 1–2. | |
| April 2006, v1.2 | <ul style="list-style-type: none"> • Updated Table 1–1. • Updated Table 1–2. | Updated numbers for receiver channels and user I/O pin counts in Table 1–2. |
| February 2006, v1.1 | <ul style="list-style-type: none"> • Updated Table 1–1. | |
| October 2005 v1.0 | Added chapter to the <i>Stratix II GX Device Handbook</i> . | |

Transceivers

Stratix® II GX devices incorporate dedicated embedded circuitry on the right side of the device, which contains up to 20 high-speed 6.375-Gbps serial transceiver channels. Each Stratix II GX transceiver block contains four full-duplex channels and supporting logic to transmit and receive high-speed serial data streams. The transceivers deliver bidirectional point-to-point data transmissions, with up to 51 Gbps (6.375 Gbps per channel) of full-duplex data transmission per transceiver block.

Figure 2–1 shows the function blocks that make up a transceiver channel within the Stratix II GX device.

Figure 2–1. Stratix II GX Transceiver Block Diagram



Notes to Figure 2–1:

- (1) n represents the number of bits in each word that need to be serialized by the transmitter portion of the PMA or have been deserialized by the receiver portion of the PMA. $n = 8, 10, 16, \text{ or } 20$.
- (2) m represents the number of bits in the word that pass between the FPGA logic and the PCS portion of the transceiver. $m = 8, 10, 16, 20, 32, \text{ or } 40$.

Transceivers within each block are independent and have their own set of dividers. Therefore, each transceiver can operate at different frequencies. Each block can select from two reference clocks to provide two clock domains that each transceiver can select from.

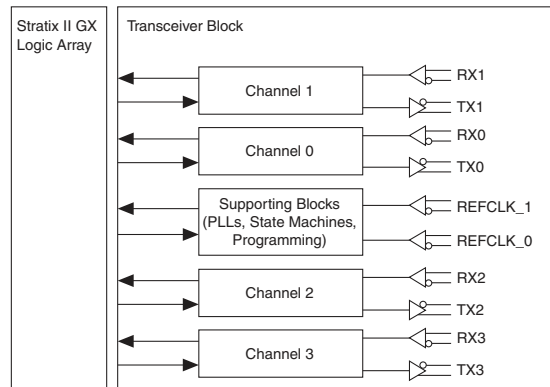
There are up to 20 transceiver channels available on a single Stratix II GX device. Table 2-1 shows the number of transceiver channels and their serial bandwidth for each Stratix II GX device.

Table 2-1. Stratix II GX Transceiver Channels

| Device | Number of Transceiver Channels | Serial Bandwidth (Full Duplex) |
|------------|--------------------------------|--------------------------------|
| EP2SGX30C | 4 | 51 Gbps |
| EP2SGX60C | 4 | 51 Gbps |
| EP2SGX30D | 8 | 102 Gbps |
| EP2SGX60D | 8 | 102 Gbps |
| EP2SGX60E | 12 | 153 Gbps |
| EP2SGX90E | 12 | 153 Gbps |
| EP2SGX90F | 16 | 204 Gbps |
| EP2SGX130G | 20 | 255 Gbps |

Figure 2-2 shows the elements of the transceiver block, including the four transceiver channels, supporting logic, and I/O buffers. Each transceiver channel consists of a receiver and transmitter. The supporting logic contains two transmitter PLLs to generate the high-speed clock(s) used by the four transmitters within that block. Each of the four transmitter channels has its own individual clock divider. The four receiver PLLs within each transceiver block generate four recovered clocks. The transceiver channels can be configured in one of the following functional modes:

- PCI Express (PIPE)
- OIF CEI PHY Interface
- SONET/SDH
- Gigabit Ethernet (GIGE)
- XAUI
- Basic (600 Mbps to 3.125 Gbps single-width mode and 1 Gbps to 6.375 Gbps double-width mode)
- SDI (HD, 3G)
- CPRI (614 Mbps, 1228 Mbps, 2456 Mbps)
- Serial RapidIO (1.25 Gbps, 2.5 Gbps, 3.125 Gbps)

Figure 2–2. Elements of the Transceiver Block

Each Stratix II GX transceiver channel consists of a transmitter and receiver. The transceivers are grouped in four and share PLL resources. Each transmitter has access to one of two PLLs. The transmitter contains the following:

- Transmitter phase compensation first-in first-out (FIFO) buffer
- Byte serializer (optional)
- 8B/10B encoder (optional)
- Serializer (parallel-to-serial converter)
- Transmitter differential output buffer

The receiver contains the following:

- Receiver differential input buffer
- Receiver lock detector and run length checker
- Clock recovery unit (CRU)
- Deserializer
- Pattern detector
- Word aligner
- Lane deskew
- Rate matcher (optional)
- 8B/10B decoder (optional)
- Byte deserializer (optional)
- Byte ordering
- Receiver phase compensation FIFO buffer

Designers can preset Stratix II GX transceiver functions using the Quartus® II software. In addition, pre-emphasis, equalization, and differential output voltage (V_{OD}) are dynamically programmable. Each Stratix II GX transceiver channel supports various loopback modes and is

capable of built-in self test (BIST) generation and verification. The ALT2GXB megafunction in the Quartus II software provides a step-by-step menu selection to configure the transceiver.

Figure 2–1 shows the block diagram for the Stratix II GX transceiver channel. Stratix II GX transceivers provide PCS and PMA implementations for all supported protocols. The PCS portion of the transceiver consists of the word aligner, lane deskew FIFO buffer, rate matcher FIFO buffer, 8B/10B encoder and decoder, byte serializer and deserializer, byte ordering, and phase compensation FIFO buffers.

Each Stratix II GX transceiver channel is also capable of BIST generation and verification in addition to various loopback modes. The PMA portion of the transceiver consists of the serializer and deserializer, the CRU, and the high-speed differential transceiver buffers that contain pre-emphasis, programmable on-chip termination (OCT), programmable voltage output differential (V_{OD}), and equalization.

Transmitter Path

This section describes the data path through the Stratix II GX transmitter. The Stratix II GX transmitter contains the following modules:

- Transmitter PLLs
- Access to one of two PLLs
- Transmitter logic array interface
- Transmitter phase compensation FIFO buffer
- Byte serializer
- 8B/10B encoder
- Serializer (parallel-to-serial converter)
- Transmitter differential output buffer

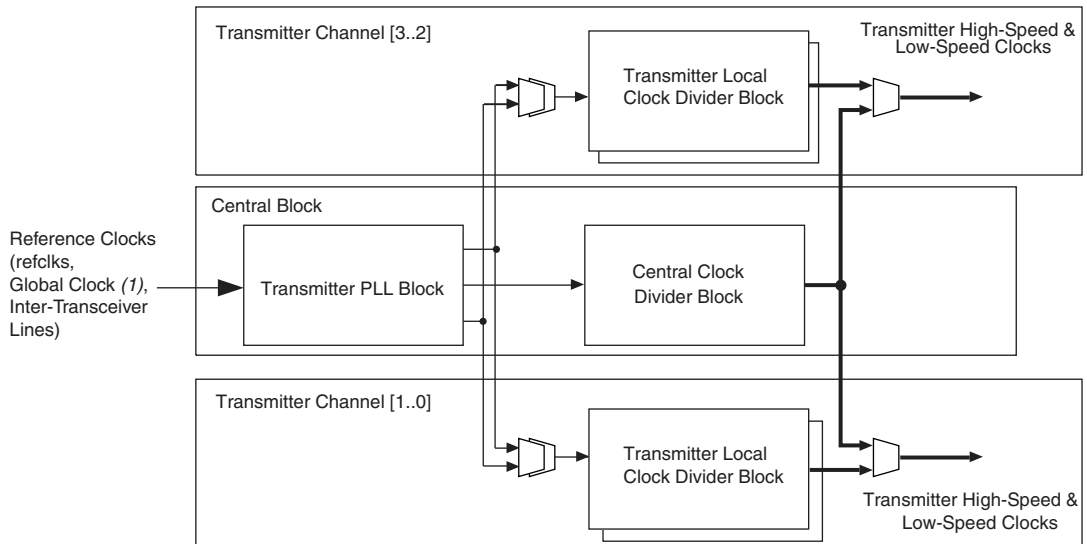
Transmitter PLLs

Each transceiver block has two transmitter PLLs which receive two reference clocks to generate timing and the following clocks:

- High-speed clock used by the serializer to transmit the high-speed differential transmitter data
- Low-speed clock to load the parallel transmitter data of the serializer

The serializer uses high-speed clocks to transmit data. The serializer is also referred to as parallel in serial out (PISO). The high-speed clock is fed to the local clock generation buffer. The local clock generation buffers divide the high-speed clock on the transmitter to a desired frequency on a per-channel basis. Figure 2–3 is a block diagram of the transmitter clocks.

Figure 2–3. Clock Distribution for the Transmitters *Note (1)*



Note to Figure 2–3:

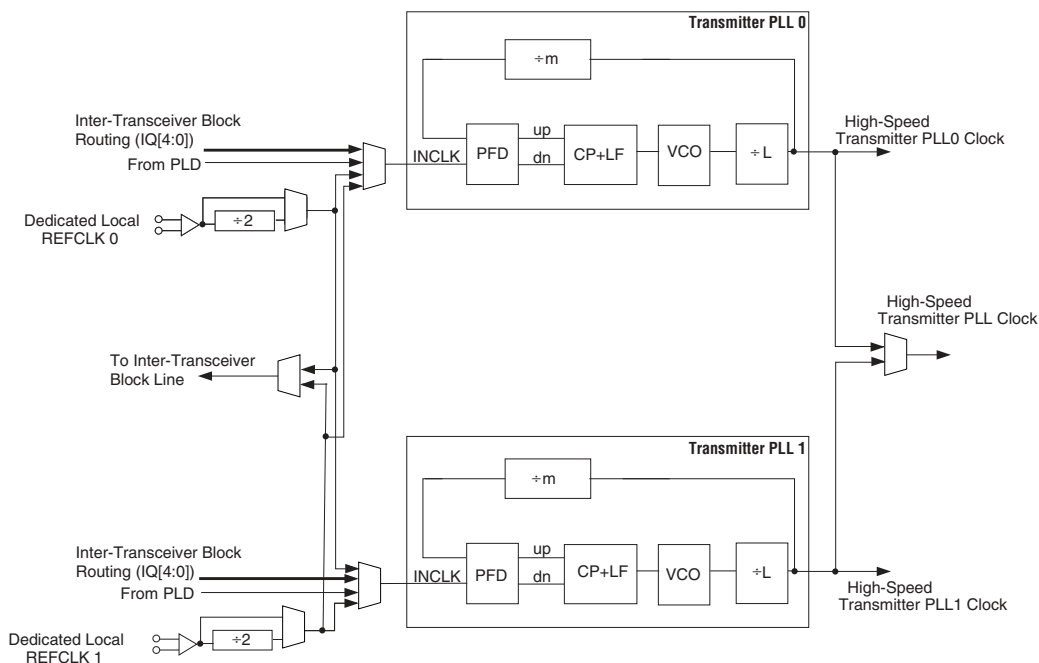
(1) The global clock line must be driven by an input pin.

The transmitter PLLs in each transceiver block clock the PMA and PCS circuitry in the transmit path. The Quartus II software automatically powers down the transmitter PLLs that are not used in the design. [Figure 2–4](#) is a block diagram of the transmitter PLL.

The transmitter phase/frequency detector references the clock from one of the following sources:

- Reference clocks
- Reference clock from the adjacent transceiver block
- Inter-transceiver block clock lines
- Global clock line driven by input pin

Two reference clocks, REFCLK0 and REFCLK1, are available per transceiver block. The inter-transceiver block bus allows multiple transceivers to use the same reference clocks. Each transceiver block has one outgoing reference clock which connects to one inter-transceiver block line. The incoming reference clock can be selected from five inter-transceiver block lines IQ[4..0] or from the global clock line that is driven by an input pin.

Figure 2–4. Transmitter PLL Block Note (1)**Note to Figure 2–4:**

(1) The global clock line must be driven by an input pin.

The transmitter PLLs support data rates up to 6.375 Gbps. The input clock frequency is limited to 622.08 MHz. An optional `p11_locked` port is available to indicate whether the transmitter PLL is locked to the reference clock. Both transmitter PLLs have a programmable loop bandwidth parameter that can be set to low, medium, or high. The loop bandwidth parameter can be statically set in the Quartus II software.

Table 2–2 lists the adjustable parameters in the transmitter PLL.

| Parameter | Specifications |
|---------------------------------|----------------------------|
| Input reference frequency range | 50 MHz to 622.08 MHz |
| Data rate support | 600 Mbps to 6.375 Gbps |
| Multiplication factor (W) | 1, 4, 5, 8, 10, 16, 20, 25 |
| Bandwidth | Low, medium, or high |

Transmitter Phase Compensation FIFO Buffer

The transmitter phase compensation FIFO buffer resides in the transceiver block at the PCS/FPGA boundary and cannot be bypassed. This FIFO buffer compensates for phase differences between the transmitter PLL clock and the clock from the PLD. After the transmitter PLL has locked to the frequency and phase of the reference clock, the transmitter FIFO buffer must be reset to initialize the read and write pointers. After FIFO pointer initialization, the PLL must remain phase locked to the reference clock.

Byte Serializer

The FPGA and transceiver block must maintain the same throughput. If the FPGA interface cannot meet the timing margin to support the throughput of the transceiver, the byte serializer is used on the transmitter and the byte deserializer is used on the receiver.

The byte serializer takes words from the FPGA interface and converts them into smaller words for use in the transceiver. The transmit data path after the byte serializer is 8, 10, 16, or 20 bits. Refer to [Table 2-3](#) for the transmitter data with the byte serializer enabled. The byte serializer can be bypassed when the data width is 8, 10, 16, or 20 bits at the FPGA interface.

Table 2-3. Transmitter Data with the Byte Serializer Enabled

| Input Data Width | Output Data Width |
|-------------------------|--------------------------|
| 16 bits | 8 bits |
| 20 bits | 10 bits |
| 32 bits | 16 bits |
| 40 bits | 20 bits |

If the byte serializer is disabled, the FPGA transmit data is passed without data width conversion.

Table 2–4 shows the data path configurations for the Stratix II GX device in single-width and double-width modes.



Refer to the section “8B/10B Encoder” on page 2–8 for a description of the single- and double-width modes.

| Parameter | Single-Width Mode | | Double-Width Mode | |
|--------------------------------------|--|---|--|---|
| | Without Byte Serialization/Deserialization | With Byte Serialization/Deserialization | Without Byte Serialization/Deserialization | With Byte Serialization/Deserialization |
| Fabric to PCS data path width (bits) | 8 or 10 | 16 or 20 | 16 or 20 | 32 or 40 |
| Data rate range (Gbps) | 0.6 to 2.5 | 0.6 to 3.125 | 1 to 5.0 | 1 to 6.375 |
| PCS to PMA data path width (bits) | 8 or 10 | 8 or 10 | 16 or 20 | 16 or 20 |
| Byte ordering (1) | | ✓ | | ✓ |
| Data symbol A (MSB) | | | | ✓ |
| Data symbol B | | ✓ | | ✓ |
| Data symbol C | | | ✓ | ✓ |
| Data symbol D (LSB) | ✓ | ✓ | ✓ | ✓ |

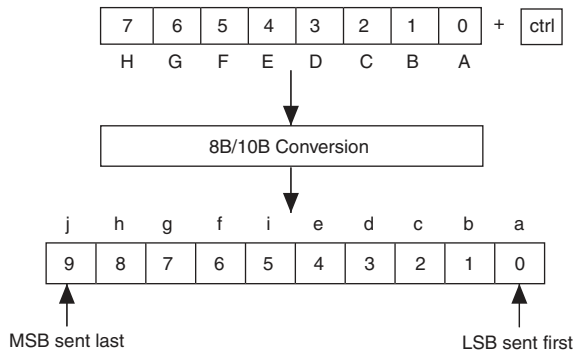
Note to Table 2–4:

(1) Designs can use byte ordering when byte serialization and deserialization are used.

8B/10B Encoder

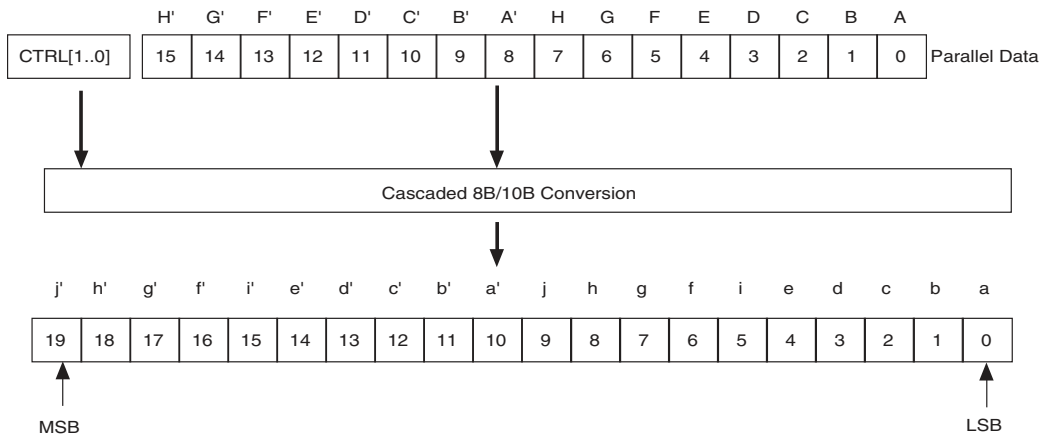
There are two different modes of operation for 8B/10B encoding. Single-width (8-bit) mode supports natural data rates from 622 Mbps to 3.125 Gbps. Double-width (16-bit cascaded) mode supports data rates above 3.125 Gbps. The encoded data has a maximum run length of five. The 8B/10B encoder can be bypassed. Figure 2–5 diagrams the 10-bit encoding process.

Figure 2-5. 8B/10B Encoding Process



In single-width mode, the 8B/10B encoder generates a 10-bit code group from the 8-bit data and 1-bit control identifier. In double-width mode, there are two 8B/10B encoders that are cascaded together and generate a 20-bit (2×10 -bit) code group from the 16-bit (2×8 -bit) data + 2-bit (2×1 -bit) control identifier. Figure 2-6 shows the 20-bit encoding process. The 8B/10B encoder conforms to the IEEE 802.3 1998 edition standards.

Figure 2-6. 16-Bit to 20-Bit Encoding Process



Upon power on or reset, the 8B/10B encoder has a negative disparity which chooses the 10-bit code from the RD-column. However, the running disparity can be changed via the `tx_forcedisp` and `tx_dispsval` ports.

Transmit State Machine

The transmit state machine operates in either PCI Express mode, XAUI mode, or GIGE mode, depending on the protocol used. The state machine is not utilized for certain protocols, such as SONET.

GIGE Mode

In GIGE mode, the transmit state machine converts all idle ordered sets (/K28.5/, /Dx.y/) to either /I1/ or /I2/ ordered sets. /I1/ consists of a negative-ending disparity /K28.5/ (denoted by /K28.5/-) followed by a neutral /D5.6/. /I2/ consists of a positive-ending disparity /K28.5/ (denoted by /K28.5/+) and a negative-ending disparity /D16.2/ (denoted by /D16.2/-). The transmit state machines do not convert any of the ordered sets to match /C1/ or /C2/, which are the configuration ordered sets. (/C1/ and /C2/ are defined by [/K28.5/, /D21.5/] and [/K28.5/, /D2.2/], respectively). Both the /I1/ and /I2/ ordered sets guarantee a negative-ending disparity after each ordered set.

XAUI Mode

The transmit state machine translates the XAUI XGMII code group to the XAUI PCS code group. Table 2–5 shows the code conversion.

| XGMII TXC | XGMII TXD | PCS Code-Group | Description |
|------------------|-------------------------------------|-------------------------------------|-------------------------|
| 0 | 00 through FF | Dxx.y | Normal data |
| 1 | 07 | K28.0 or K28.3 or K28.5 | Idle in I |
| 1 | 07 | K28.5 | Idle in T |
| 1 | 9C | K28.4 | Sequence |
| 1 | FB | K27.7 | Start |
| 1 | FD | K29.7 | Terminate |
| 1 | FE | K30.7 | Error |
| 1 | See IEEE 802.3 reserved code groups | See IEEE 802.3 reserved code groups | Reserved code groups |
| 1 | Other value | K30.7 | Invalid XGMII character |

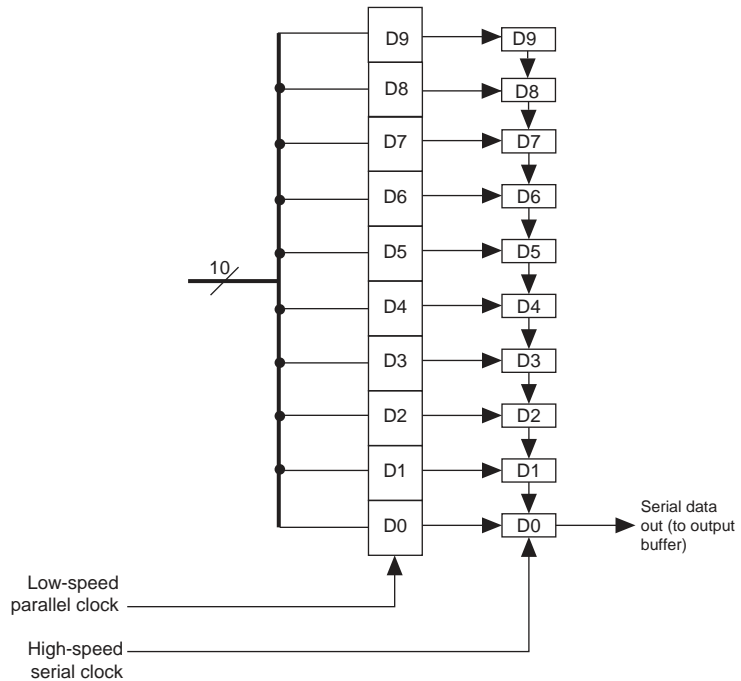
The XAUI PCS idle code groups, /K28.0/ (/R/) and /K28.5/ (/K/), are automatically randomized based on a PRBS7 pattern with an $x^7 + x^6 + 1$ polynomial. The /K28.3/ (/A/) code group is automatically generated between 16 and 31 idle code groups. The idle randomization on the /A/, /K/, and /R/ code groups is done automatically by the transmit state machine.

Serializer (Parallel-to-Serial Converter)

The serializer converts the parallel 8, 10, 16, or 20-bit data into a serial data bit stream, transmitting the least significant bit (LSB) first. The serialized data stream is then fed to the high-speed differential transmit buffer.

Figure 2-7 is a diagram of the serializer.

Figure 2-7. Serializer *Note (1)*



Note to Figure 2-7:

(1) This is a 10-bit serializer. The serializer can also convert 8, 16, and 20 bits of data.

Transmit Buffer

The Stratix II GX transceiver buffers support the 1.2- and 1.5-V PCML I/O standard at rates up to 6.375 Gbps. The common mode voltage (V_{CM}) of the output driver is programmable. The following V_{CM} values are available when the buffer is in 1.2- and 1.5-V PCML.

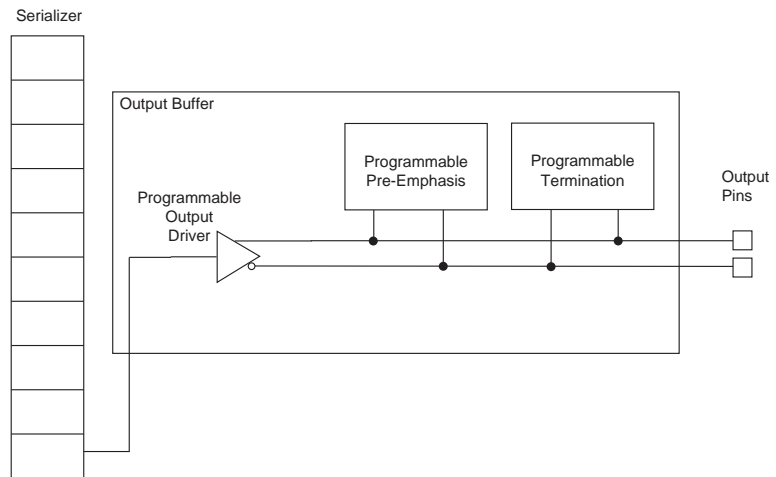
- $V_{CM} = 0.6$ V
- $V_{CM} = 0.7$ V



Refer to the *Stratix II GX Transceiver Architecture Overview* chapter in volume 2 of the *Stratix II GX Handbook*.

The output buffer, as shown in [Figure 2–8](#), is directly driven by the high-speed data serializer and consists of a programmable output driver, a programmable pre-emphasis circuit, a programmable termination, and a programmable V_{CM} .

Figure 2–8. Output Buffer



Programmable Output Driver

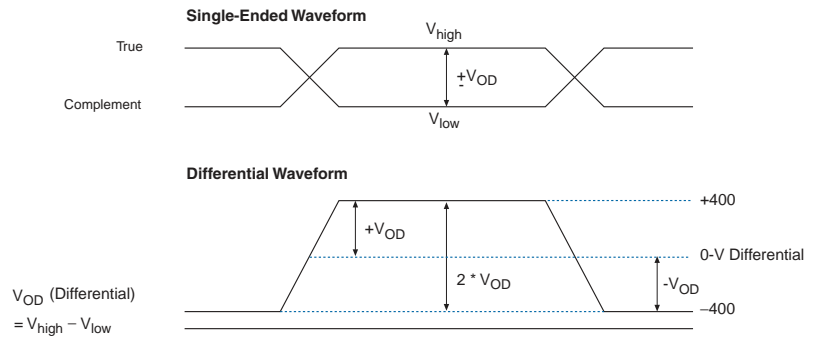
The programmable output driver can be set to drive out differentially 200 to 1,400 mV. The differential output voltage (V_{OD}) can be changed dynamically, or statically set by using the ALT2GXB megafunction or through I/O pins.

The output driver may be programmed with four different differential termination values:

- 100 Ω
- 120 Ω
- 150 Ω
- External termination

Differential signaling conventions are shown in Figure 2–9. The differential amplitude represents the value of the voltage between the true and complement signals. Peak-to-peak differential voltage is defined as $2 \times (V_{\text{HIGH}} - V_{\text{LOW}}) = 2 \times$ single-ended voltage swing. The common mode voltage is the average of V_{high} and V_{low} .

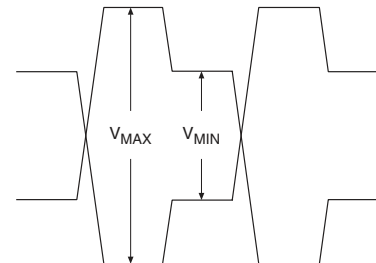
Figure 2–9. Differential Signaling



Programmable Pre-Emphasis

The programmable pre-emphasis module controls the output driver to boost the high frequency components, and compensate for losses in the transmission medium, as shown in Figure 2–10. The pre-emphasis is set statically using the ALT2GXB megafunction or dynamically through the dynamic reconfiguration controller.

Figure 2–10. Pre-Emphasis Signaling



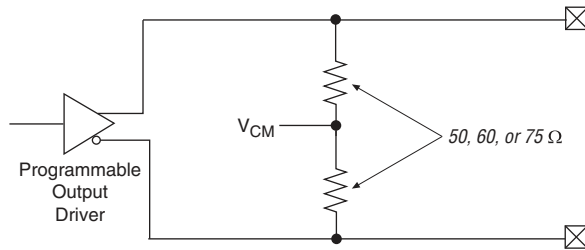
$$\text{Pre-Emphasis \%} = \left(\frac{V_{\text{MAX}}}{V_{\text{MIN}}} - 1 \right) \times 100$$

Pre-emphasis percentage is defined as $(V_{MAX}/V_{MIN} - 1) \times 100$, where V_{MAX} is the differential emphasized voltage (peak-to-peak) and V_{MIN} is the differential steady-state voltage (peak-to-peak).

Programmable Termination

The programmable termination can be statically set in the Quartus II software. The values are 100 Ω , 120 Ω , 150 Ω , and external termination. [Figure 2-11](#) shows the setup for programmable termination.

Figure 2-11. Programmable Transmitter Terminations



PCI Express Receiver Detect

The Stratix II GX transmitter buffer has a built-in receiver detection circuit for use in PIPE mode. This circuit provides the ability to detect if there is a receiver downstream by sending out a pulse on the channel and monitoring the reflection. This mode requires the transmitter buffer to be tri-stated (in electrical idle mode).

PCI Express Electric Idles (or Individual Transmitter Tri-State)

The Stratix II GX transmitter buffer supports PCI Express electrical idles. This feature is only active in PIPE mode. The `tx_forceelectricidle` port puts the transmitter buffer in electrical idle mode. This port is available in all PCI Express power-down modes and has specific usage in each mode.

Receiver Path

This section describes the data path through the Stratix II GX receiver. The Stratix II GX receiver consists of the following blocks:

- Receiver differential input buffer
- Receiver PLL lock detector, signal detector, and run length checker
- Clock/data recovery (CRU) unit
- Deserializer
- Pattern detector
- Word aligner

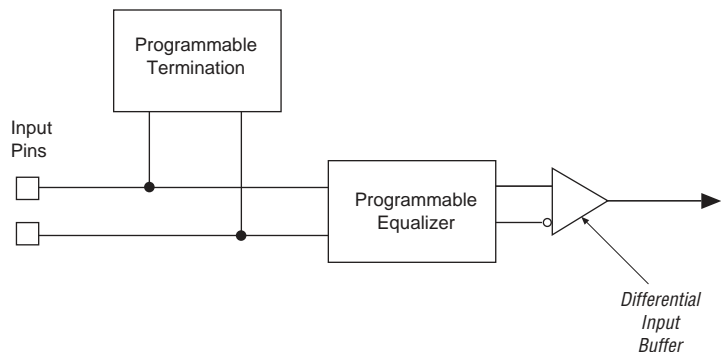
- Lane deskew
- Rate matcher
- 8B/10B decoder
- Byte deserializer
- Byte ordering
- Receiver phase compensation FIFO buffer

Receiver Input Buffer

The Stratix II GX receiver input buffer supports the 1.2-V and 1.5-V PCML I/O standard at rates up to 6.375 Gbps. The common mode voltage of the receiver input buffer is programmable between 0.85 V and 1.2 V. You must select the 0.85 V common mode voltage for AC- and DC-coupled PCML links and the 1.2 V common mode voltage for DC-coupled LVDS links.

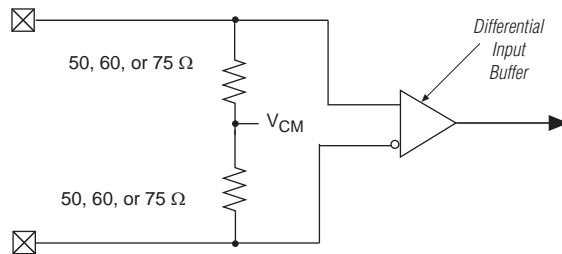
The receiver has programmable on-chip 100-, 120-, or 150- Ω differential termination for different protocols, as shown in [Figure 2–12](#). The receiver's internal termination can be disabled if external terminations and biasing are provided. The receiver and transmitter differential termination resistances can be set independently of each other.

Figure 2–12. Receiver Input Buffer

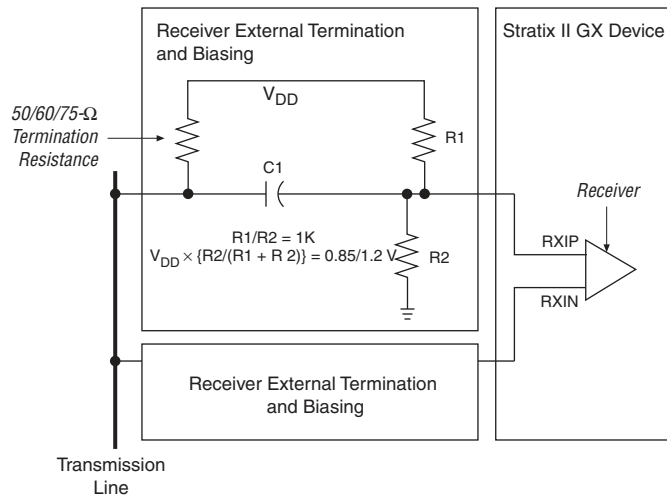


Programmable Termination

The programmable termination can be statically set in the Quartus II software. [Figure 2–13](#) shows the setup for programmable receiver termination. The termination can be disabled if external termination is provided.

Figure 2–13. Programmable Receiver Termination

If a design uses external termination, the receiver must be externally terminated and biased to 0.85 V or 1.2 V. [Figure 2–14](#) shows an example of an external termination and biasing circuit.

Figure 2–14. External Termination and Biasing Circuit

Programmable Equalizer

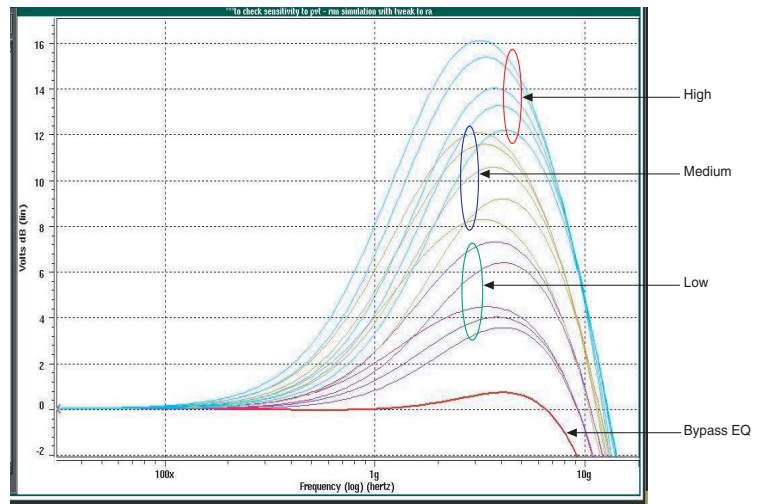
The Stratix II GX receivers provide a programmable receive equalization feature to compensate the effects of channel attenuation for high-speed signaling. PCB traces carrying these high-speed signals have low-pass filter characteristics. The impedance mismatch boundaries can also cause signal degradation. The equalization in the receiver diminishes the lossy attenuation effects of the PCB at high frequencies.



The Stratix II GX receivers also have adaptive equalization capability that adjusts the equalization levels to compensate for changing link characteristics. The adaptive equalization can be powered down dynamically after it selects the appropriate equalization levels.

The receiver equalization circuit is comprised of a programmable amplifier. Each stage is a peaking equalizer with a different center frequency and programmable gain. This allows varying amounts of gain to be applied, depending on the overall frequency response of the channel loss. Channel loss is defined as the summation of all losses through the PCB traces, vias, connectors, and cables present in the physical link. [Figure 2-15](#) shows the frequency response for the 16 programmable settings allowed by the Quartus II software for Stratix II GX devices.

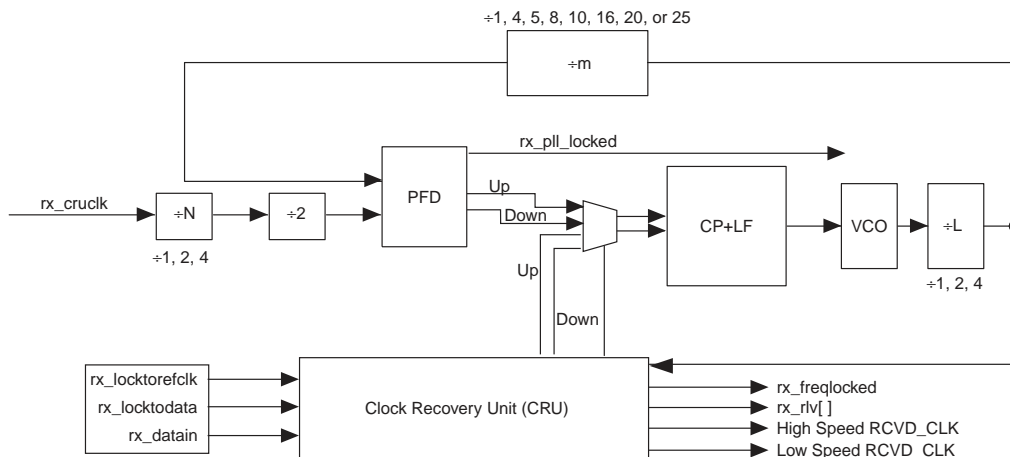
Figure 2-15. Frequency Response



Receiver PLL and CRU

Each transceiver block has four receiver PLLs, lock detectors, signal detectors, run length checkers, and CRU units, each of which is dedicated to a receive channel. If the receive channel associated with a particular receiver PLL or CRU is not used, the receiver PLL and CRU are powered down for the channel. [Figure 2-16](#) shows the receiver PLL and CRU circuits.

Figure 2–16. Receiver PLL and CRU



The receiver PLLs and CRUs can support frequencies up to 6.375 Gbps. The input clock frequency is limited to the full clock range of 50 to 622 MHz but only when using REFCLK0 or REFCLK1. An optional RX_PLL_LOCKED port is available to indicate whether the PLL is locked to the reference clock. The receiver PLL has a programmable loop bandwidth which can be set to low, medium, or high. The Quartus II software can statically set the loop bandwidth parameter.

All the parameters listed are programmable in the Quartus II software. The receiver PLL has the following features:

- Operates from 600 Mbps to 6.375 Gbps.
- Uses a reference clock between 50 MHz and 622.08 MHz.
- Programmable bandwidth settings: low, medium, and high.
- Programmable rx_locktorefclk (forces the receiver PLL to lock to the reference clock) and rx_locktodata (forces the receiver PLL to lock to the data).
- The voltage-controlled oscillator (VCO) operates at half rate and has two modes. These modes are for low or high frequency operation and provide optimized phase-noise performance.
- Programmable frequency multiplication W of 1, 4, 5, 8, 10, 16, 20, and 25. Not all settings are supported for any particular frequency.
- Two lock indication signals are provided. They are found in PFD mode (lock-to-reference clock), and PD (lock-to-data).

The CRU has a built-in switchover circuit to select whether the PLL VCO is aligned by the reference clock or the data. The optional port `rx_freqlocked` monitors when the CRU is in locked-to-data mode.

In the automatic mode, the CRU PLL must be within the prescribed PPM frequency threshold setting of the CRU reference clock for the CRU to switch from locked-to-reference to locked-to-data mode.

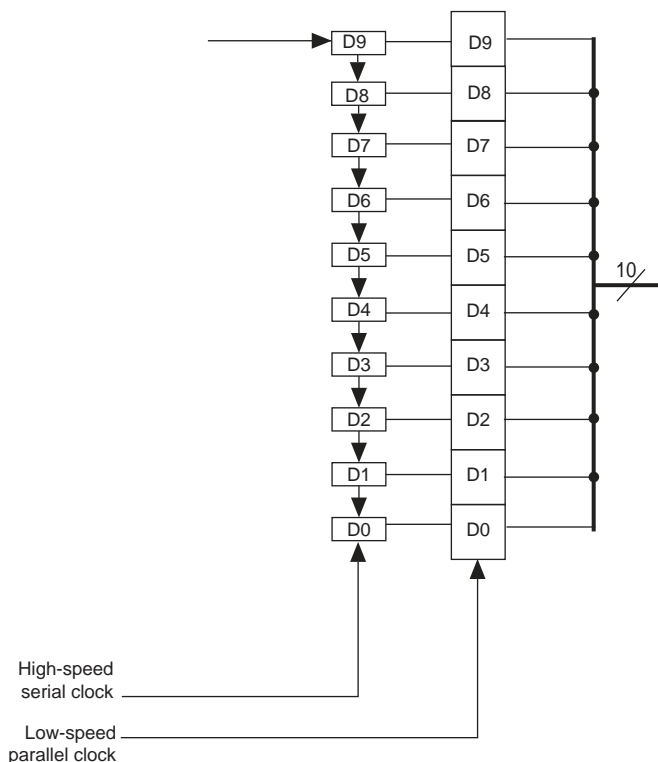
The automatic switchover circuit can be overridden by using the optional ports `rx_locktorefclk` and `rx_locktodata`. [Table 2-6](#) shows the possible combinations of these two signals.

| <i>Table 2-6. Receiver Lock Combinations</i> | | |
|--|------------------------------|--------------------|
| <code>rx_locktodata</code> | <code>rx_locktorefclk</code> | VCO (Lock to Mode) |
| 0 | 0 | Auto |
| 0 | 1 | Reference clock |
| 1 | x | Data |

If the `rx_locktorefclk` and `rx_locktodata` ports are not used, the default is auto mode.

Deserializer (Serial-to-Parallel Converter)

The deserializer converts a serial bitstream into 8, 10, 16, or 20 bits of parallel data. The deserializer receives the LSB first. [Figure 2-17](#) shows the deserializer.

Figure 2–17. Deserializer Note (1)**Note to Figure 2–17:**

(1) This is a 10-bit deserializer. The deserializer can also convert 8, 16, or 20 bits of data.

Word Aligner

The deserializer block creates 8-, 10-, 16-, or 20-bit parallel data. The deserializer ignores protocol symbol boundaries when converting this data. Therefore, the boundaries of the transferred words are arbitrary. The word aligner aligns the incoming data based on specific byte or word boundaries. The word alignment module is clocked by the local receiver recovered clock during normal operation. All the data and programmed patterns are defined as big-endian (most significant word followed by least significant word). Most-significant-bit-first protocols such as SONET/SDH should reverse the bit order of word align patterns programmed.

This module detects word boundaries for the 8B/10B-based protocols, SONET, 16-bit, and 20-bit proprietary protocols. This module is also used to align to specific programmable patterns in PRBS7/23 test mode.

Pattern Detection

The programmable pattern detection logic can be programmed to align word boundaries using a single 7-, 8-, 10-, 16-, 20, or 32-bit pattern. The pattern detector can either do an exact match, or match the exact pattern and the complement of a given pattern. Once the programmed pattern is found, the data stream is aligned to have the pattern on the LSB portion of the data output bus.

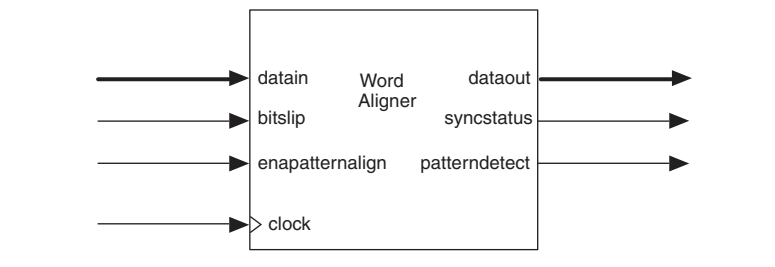
XAUI, GIGE, PCI Express, and Serial RapidIO standards have embedded state machines for symbol boundary synchronization. These standards use K28.5 as their 10-bit programmed comma pattern. Each of these standards uses different algorithms before signaling symbol boundary acquisition to the FPGA.

The pattern detection logic searches from the LSB to the most significant bit (MSB). If multiple patterns are found within the search window, the pattern in the lower portion of the data stream (corresponding to the pattern received earlier) is aligned and the rest of the matching patterns are ignored.

Once a pattern is detected and the data bus is aligned, the word boundary is locked. The two detection status signals (`rx_syncstatus` and `rx_patterndetect`) indicate that an alignment is complete.

Figure 2–18 is a block diagram of the word aligner.

Figure 2–18. Word Aligner



Control and Status Signals

The `rx_enapatternalign` signal is the FPGA control signal that enables word alignment in non-automatic modes. The `rx_enapatternalign` signal is not used in automatic modes (PCI Express, XAUI, GIGE, CPRI, and Serial RapidIO).

In manual alignment mode, after the `rx_enapatternalign` signal is activated, the `rx_syncstatus` signal goes high for one parallel clock cycle to indicate that the alignment pattern has been detected and the word boundary has been locked. If the `rx_enapatternalign` is deactivated, the `rx_syncstatus` signal acts as a re-synchronization signal to signify that the alignment pattern has been detected but not locked on a different word boundary.

When using the synchronization state machine, the `rx_syncstatus` signal indicates the link status. If the `rx_syncstatus` signal is high, link synchronization is achieved. If the `rx_syncstatus` signal is low, synchronization has not yet been achieved, or there were enough code group errors to lose synchronization.

In some modes, the `rx_enapatternalign` signal can be configured to operate as a rising edge signal.



For more information on manual alignment modes, refer to the *Stratix II GX Device Handbook*, volume 2.

When the `rx_enapatternalign` signal is sensitive to the rising edge, each rising edge triggers a new boundary alignment search, clearing the `rx_syncstatus` signal.

The `rx_patterndetect` signal pulses high during a new alignment, and also whenever the alignment pattern occurs on the current word boundary.

SONET/SDH

In all the SONET/SDH modes, you can configure the word aligner to either align to A1A2 or A1A1A2A2 patterns. Once the pattern is found, the word boundary is aligned and the word aligner asserts the `rx_patterndetect` signal for one clock cycle.

Programmable Run Length Violation

The word aligner supports a programmable run length violation counter. Whenever the number of the continuous '0' (or '1') exceeds a user programmable value, the `rx_rlv` signal goes high for a minimum pulse width of two recovered clock cycles. The maximum run values supported are shown in [Table 2-7](#).

| Mode | PMA Serialization | | | |
|--------------|-------------------|--------|--------|--------|
| | 8 Bit | 10 Bit | 16 Bit | 20 Bit |
| Single-Width | 128 | 160 | — | — |
| Double-Width | — | — | 512 | 640 |

Running Disparity Check

The running disparity error `rx_disperr` and running disparity value `rx_runningdisp` are sent along with aligned data from the 8B/10B decoder to the FPGA. You can ignore or act on the reported running disparity value and running disparity error signals.

Bit-Slip Mode

The word aligner can operate in either pattern detection mode or in bit-slip mode.

The bit-slip mode provides the option to manually shift the word boundary through the FPGA. This feature is useful for:

- Longer synchronization patterns than the pattern detector can accommodate
- Scrambled data stream
- Input stream consisting of over-sampled data

This feature can be applied at 10-bit and 16-bit data widths.

The word aligner outputs a word boundary as it is received from the analog receiver after reset. You can examine the word and search its boundary in the FPGA. To do so, assert the `rx_bitslip` signal. The `rx_bitslip` signal should be toggled and held constant for at least two FPGA clock cycles.

For every rising edge of the `rx_bitslip` signal, the current word boundary is slipped by one bit. Every time a bit is slipped, the bit received earliest is lost. If bit slipping shifts a complete round of bus width, the word boundary is back to the original boundary.

The rx_syncstatus signal is not available in bit-slipping mode.

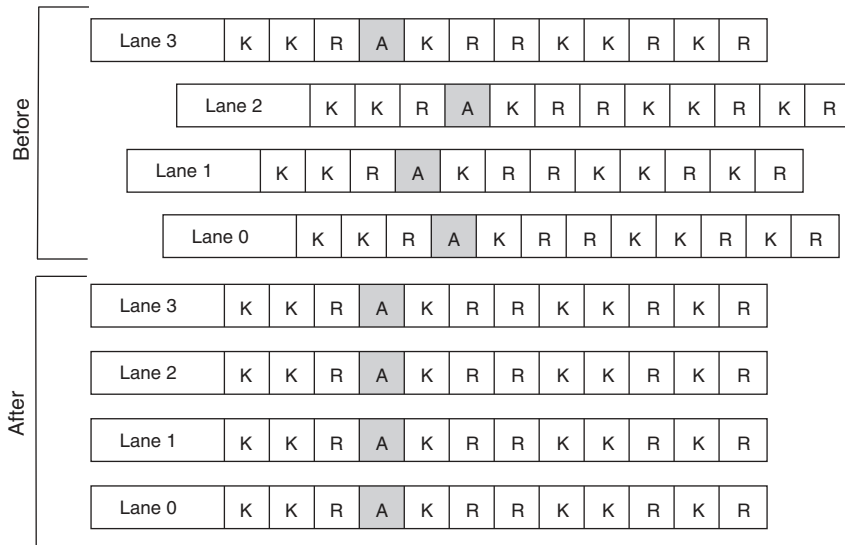
Channel Aligner

The channel aligner is available only in XAUI mode and aligns the signals of all four channels within a transceiver. The channel aligner follows the IEEE 802.3ae, clause 48 specification for channel bonding.

The channel aligner is a 16-word FIFO buffer with a state machine controlling the channel bonding process. The state machine looks for an /A/ (/K28.3/) in each channel, and aligns all the /A/ code groups in the transceiver. When four columns of /A/ (denoted by //A//) are detected, the rx_channelaligned signal goes high, signifying that all the channels in the transceiver have been aligned. The reception of four consecutive misaligned /A/ code groups restarts the channel alignment sequence and sends the rx_channelaligned signal low.

Figure 2–19 shows misaligned channels before the channel aligner and the aligned channels after the channel aligner.

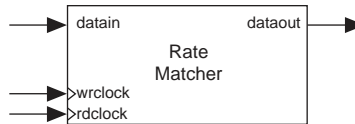
Figure 2–19. Before and After the Channel Aligner



Rate Matcher

Rate matcher is available in Basic, PCI Express, XAUI, and GIGE modes and consists of a 20-word deep FIFO buffer and a FIFO controller. [Figure 2–20](#) shows the implementation of the rate matcher in the Stratix II GX device.

Figure 2–20. Rate Matcher



In a multi-crystal environment, the rate matcher compensates for up to a ± 300 -PPM difference between the source and receiver clocks. [Table 2–8](#) shows the standards supported and the PPM for the rate matcher tolerance.

Table 2–8. Rate Matcher PPM Support *Note (1)*

| Standard | PPM |
|--------------------|-----------|
| XAUI | ± 100 |
| PCI Express (PIPE) | ± 300 |
| GIGE | ± 100 |
| Basic Double-Width | ± 300 |

Note to Table 2–8:

(1) Refer to the [Stratix II GX Transceiver User Guide](#) for the Altera®-defined scheme.

Basic Mode

In Basic mode, you can program the skip and control pattern for rate matching. In single-width Basic mode, there is no restriction on the deletion of a skip character in a cluster. The rate matcher deletes the skip characters as long as they are available. For insertion, the rate matcher inserts skip characters such that the number of skip characters at the output of rate matcher does not exceed five. In double-width mode, the rate matcher deletes skip character when they appear as pairs in the upper and lower bytes. There are no restrictions on the number of skip characters that are deleted. The rate matcher inserts skip characters as pairs.

GIGE Mode

In GIGE mode, the rate matcher adheres to the specifications in clause 36 of the IEEE 802.3 documentation for idle additions or removals. The rate matcher performs clock compensation only on /I2/ ordered sets, composed of a /K28.5/+ followed by a /D16.2/-. The rate matcher does not perform clock compensation on any other ordered set combinations. An /I2/ is added or deleted automatically based on the number of words in the FIFO buffer. A K28.4 is given at the control and data ports when the FIFO buffer is in an overflow or underflow condition.

XAUI Mode

In XAUI mode, the rate matcher adheres to clause 48 of the IEEE 802.3ae specification for clock rate compensation. The rate matcher performs clock compensation on columns of /R/ (/K28.0/), denoted by //R//. An //R// is added or deleted automatically based on the number of words in the FIFO buffer.

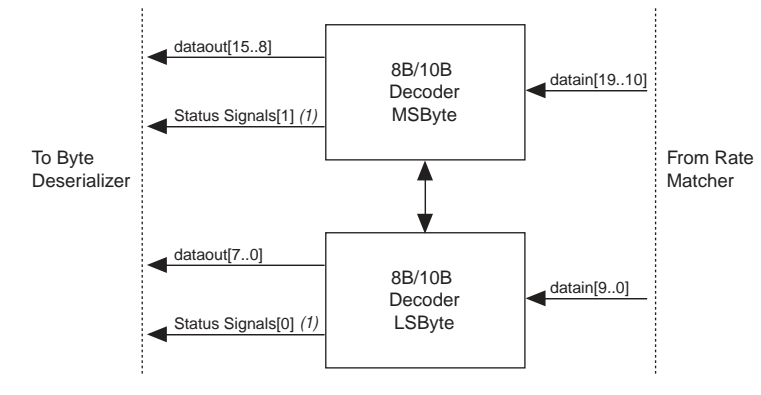
PCI Express Mode

PCI Express mode operates at a data rate of 2.5 Gbps, and supports lane widths of $\times 1$, $\times 2$, $\times 4$, and $\times 8$. The rate matcher can support up to ± 300 -PPM differences between the upstream transmitter and the receiver. The rate matcher looks for the skip ordered sets (SOS), which usually consist of a /K28.5/ comma followed by three /K28.0/ skip characters. The rate matcher deletes or inserts skip characters when necessary to prevent the rate matching FIFO buffer from overflowing or underflowing.

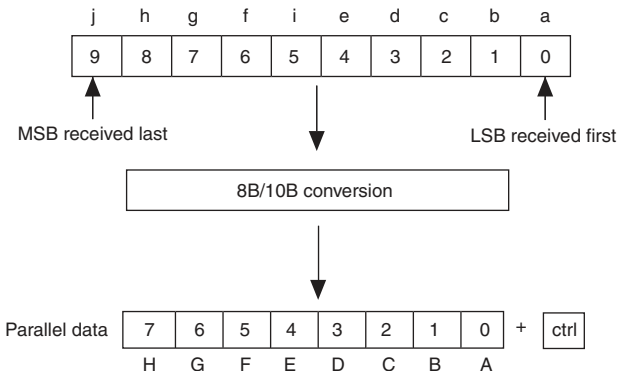
The Stratix II GX rate matcher in PCI Express mode has FIFO overflow and underflow protection. In the event of a FIFO overflow, the rate matcher deletes any data after the overflow condition to prevent FIFO pointer corruption until the rate matcher is not full. In an underflow condition, the rate matcher inserts 9'h1FE (/K30.7/) until the FIFO is not empty. These measures ensure that the FIFO can gracefully exit the overflow and underflow condition without requiring a FIFO reset.

8B/10B Decoder

The 8B/10B decoder (Figure 2-21) is part of the Stratix II GX transceiver digital blocks (PCS) and lies in the receiver path between the rate matcher and the byte deserializer blocks. The 8B/10B decoder operates in single-width and double-width modes, and can be bypassed if the 8B/10B decoding is not necessary. In single-width mode, the 8B/10B decoder restores the 8-bit data + 1-bit control identifier from the 10-bit code. In double-width mode, there are two 8B/10B decoders in parallel, which restores the 16-bit (2×8 -bit) data + 2-bit (2×1 -bit) control identifier from the 20-bit (2×10 -bit) code. This 8B/10B decoder conforms to the IEEE 802.3 1998 edition standards.

Figure 2–21. 8B/10B Decoder

The 8B/10B decoder in single-width mode translates the 10-bit encoded data into the 8-bit equivalent data or control code. The 10-bit code received must be from the supported Dx.y or Kx.y list with the proper disparity or error flags asserted. All 8B/10B control signals, such as disparity error or control detect, are pipelined with the data and edge-aligned with the data. [Figure 2–22](#) shows how the 10-bit symbol is decoded in the 8-bit data + 1-bit control indicator.

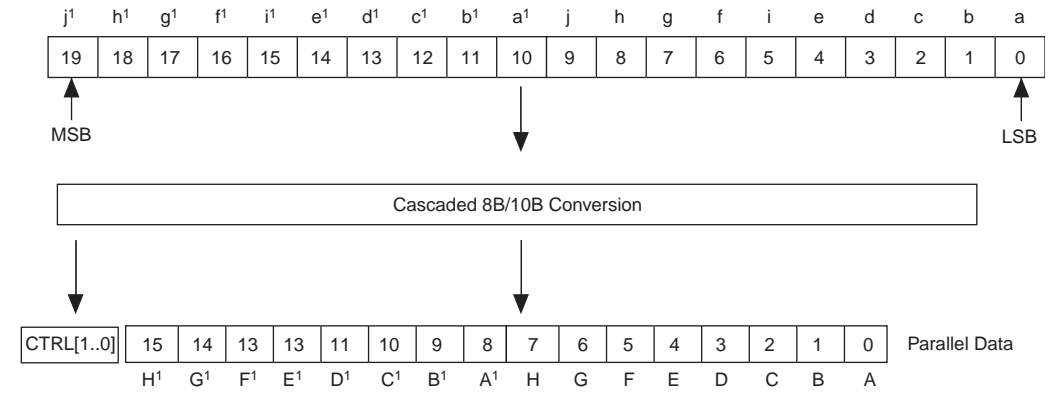
Figure 2–22. 8B/10B Decoder Conversion

The 8B/10B decoder in double-width mode translates the 20-bit (2×10 -bits) encoded code into the 16-bit (2×8 -bits) equivalent data or control code. The 20-bit upper and lower symbols received must be from the supported Dx.y or Kx.y list with the proper disparity or error flags

asserted. All 8B/10B control signals, such as disparity error or control detect, are pipelined with the data in the Stratix II GX receiver block and are edge aligned with the data.

Figure 2–23 shows how the 20-bit code is decoded to the 16-bit data + 2-bit control indicator.

Figure 2–23. 20-Bit to 16-Bit Decoding Process



There are two optional error status ports available in the 8B/10B decoder, `rx_errdetect` and `rx_dispersr`. These status signals are aligned with the code group in which the error occurred.

Receiver State Machine

The receiver state machine operates in Basic, GIGE, PCI Express, and XAUI modes. In GIGE mode, the receiver state machine replaces invalid code groups with K30.7. In XAUI mode, the receiver state machine translates the XAUI PCS code group to the XAUI XGMII code group.

Byte Deserializer

The byte deserializer widens the transceiver data path before the FPGA interface. This reduces the rate at which the received data needs to be clocked at in the FPGA logic. The byte deserializer block is available in both single- and double-width modes.

The byte deserializer converts the one- or two-byte interface into a two- or four-byte-wide data path from the transceiver to the FPGA logic (see Table 2–9). The FPGA interface has a limit of 250 MHz, so the byte deserializer is needed to widen the bus width at the FPGA interface and

reduce the interface speed. For example, at 6.375 Gbps, the transceiver logic has a double-byte-wide data path that runs at 318.75 MHz in a $\times 20$ deserializer factor, which is above the maximum FPGA interface speed. When using the byte deserializer, the FPGA interface width doubles to 40-bits (36-bits when using the 8B/10B encoder) and the interface speed reduces to 159.375 MHz.

Table 2–9. Byte Deserializer Input and Output Widths

| Input Data Width (Bits) | Deserialized Output Data Width to the FPGA (Bits) |
|-------------------------|---|
| 20 | 40 |
| 16 | 32 |
| 10 | 20 |
| 8 | 16 |

Byte Ordering Block

The byte ordering block shifts the byte order. A pre-programmed byte in the input data stream is detected and placed in the least significant byte of the output stream. Subsequent bytes start appearing in the byte positions following the LSB. The byte ordering block inserts the programmed PAD characters to shift the byte order pattern to the LSB.

Based on the setting in the MegaWizard® Plug-In Manager, the byte ordering block can be enabled either by the `rx_syncstatus` signal or by the `rx_enabyteord` signal from the PLD. When the `rx_syncstatus` signal is used as enable, the byte ordering block reorders the data only for the first occurrence of the byte order pattern that is received after word alignment is completed. You must assert `rx_digitalreset` to perform byte ordering again. However, when the byte ordering block is controlled by `rx_enabyteord`, the byte ordering block can be controlled by the PLD logic dynamically. When you create your functional mode in the MegaWizard, you can select byte ordering block only if rate matcher is not selected.

Receiver Phase Compensation FIFO Buffer

The receiver phase compensation FIFO buffer resides in the transceiver block at the FPGA boundary and cannot be bypassed. This FIFO buffer compensates for phase differences and clock tree timing skew between the receiver clock domain within the transceiver and the receiver FPGA clock after it has transferred to the FPGA.

When the FIFO pointers initialize, the receiver domain clock must remain phase locked to receiver FPGA clock.

After resetting the receiver FIFO buffer, writing to the receiver FIFO buffer begins and continues on each parallel clock. The phase compensation FIFO buffer is eight words deep for PIPE mode and four words deep for all other modes.

Loopback Modes

The Stratix II GX transceiver has built-in loopback modes for debugging and testing. The loopback modes are configured in the Stratix II GX ALT2GXB megafunction in the Quartus II software. The available loopback modes are:

- Serial loopback
- Parallel loopback
- Reverse serial loopback
- Reverse serial loopback (pre-CDR)
- PCI Express PIPE reverse parallel loopback (available only in PIPE mode)

Serial Loopback

The serial loopback mode exercises all the transceiver logic, except for the input buffer. Serial loopback is available for all non-PIPE modes. The loopback function is dynamically enabled through the `rx_serialpbken` port on a channel-by-channel basis.

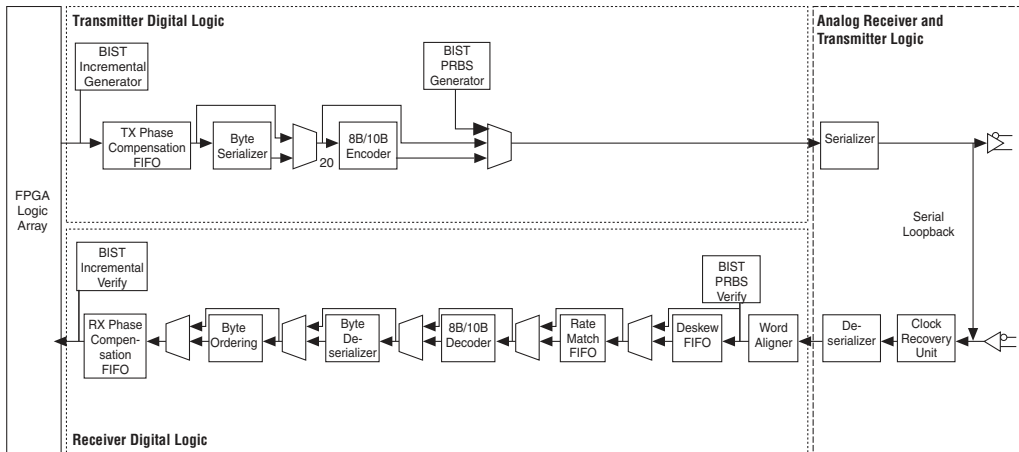
In serial loopback mode, the data on the transmit side is sent by the PLD. A separate mode is available in the ALT2GXB megafunction under Basic protocol mode, in which PRBS data is generated and verified internally in the transceiver. The PRBS patterns available in this mode are shown in [Table 2–10](#).

[Table 2–10](#) shows the BIST data output and verifier alignment pattern.

| Table 2–10. BIST Data Output and Verifier Alignment Pattern | | | | | |
|--|--------------------|----------------------------|---------------|---------------|---------------|
| Pattern | Polynomial | Parallel Data Width | | | |
| | | 8-Bit | 10-Bit | 16-Bit | 20-Bit |
| PRBS-7 | $x^7 + x^6 + 1$ | | | | ✓ |
| PRBS-10 | $x^{10} + x^7 + 1$ | | ✓ | | |

Figure 2–24 shows the data path in serial loopback mode.

Figure 2–24. Stratix II GX Block in Serial Loopback Mode with BIST and PRBS



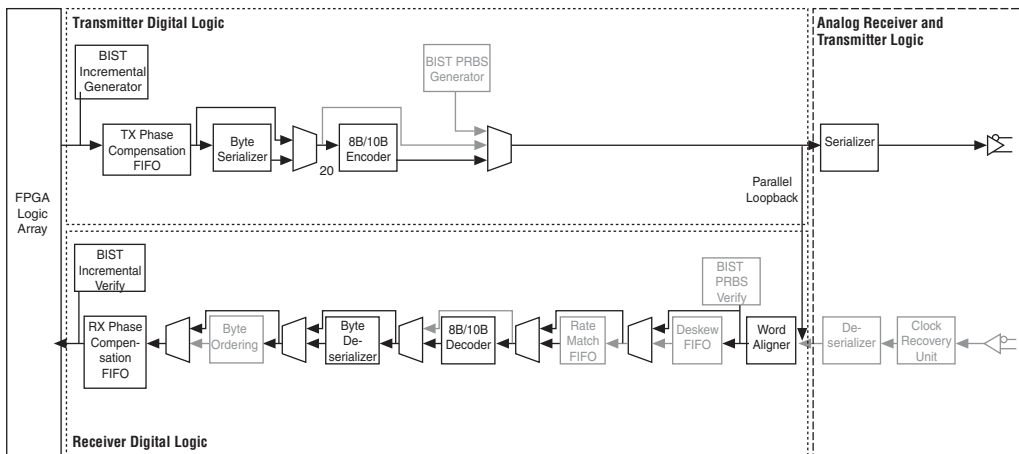
Parallel Loopback

The parallel loopback mode exercises the digital logic portion of the transceiver data path. The analog portions are not used in this loopback path, and the received high-speed serial data is not retimed. This protocol is available as one of the sub-protocols under Basic mode and can be used only for Basic double-width mode.

In this loopback mode, the data from the internally available BIST generator is transmitted. The data is looped back after the end of PCS and before the PMA. On the receive side, an internal BIST verifier checks for errors. This loopback enables you to verify the PCS block.

Figure 2–25 shows the data path in parallel loopback mode.

Figure 2–25. Stratix II GX Block in Parallel Loopback Mode

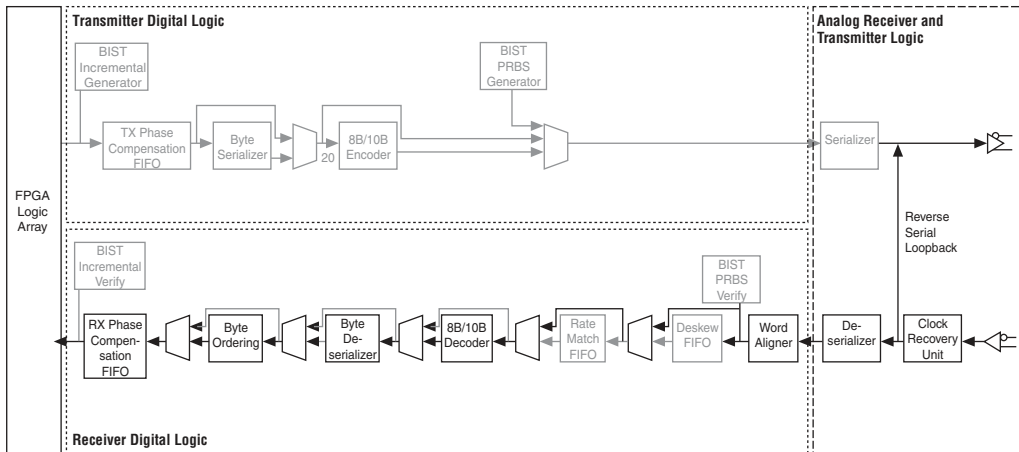


Reverse Serial Loopback

The reverse serial loopback mode uses the analog portion of the transceiver. An external source (pattern generator or transceiver) generates the source data. The high-speed serial source data arrives at the high-speed differential receiver input buffer, passes through the CRU unit, and the retimed serial data is looped back and transmitted through the high-speed differential transmitter output buffer.

Figure 2–26 shows the data path in reverse serial loopback mode.

Figure 2–26. Stratix II GX Block in Reverse Serial Loopback Mode

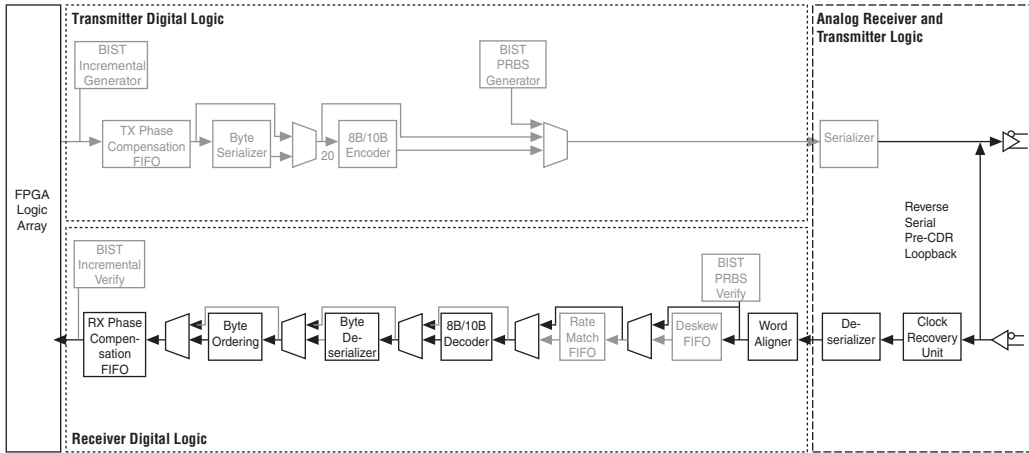


Reverse Serial Pre-CDR Loopback

The reverse serial pre-CDR loopback mode uses the analog portion of the transceiver. An external source (pattern generator or transceiver) generates the source data. The high-speed serial source data arrives at the high-speed differential receiver input buffer, loops back before the CRU unit, and is transmitted through the high-speed differential transmitter output buffer. It is for test or verification use only to verify the signal being received after the gain and equalization improvements of the input buffer. The signal at the output is not exactly what is received since the signal goes through the output buffer and the VOD is changed to the VOD setting level. The pre-emphasis settings have no effect.

Figure 2–27 show the Stratix II GX block in reverse serial pre-CDR loopback mode.

Figure 2–27. Stratix II GX Block in Reverse Serial Pre-CDR Loopback Mode

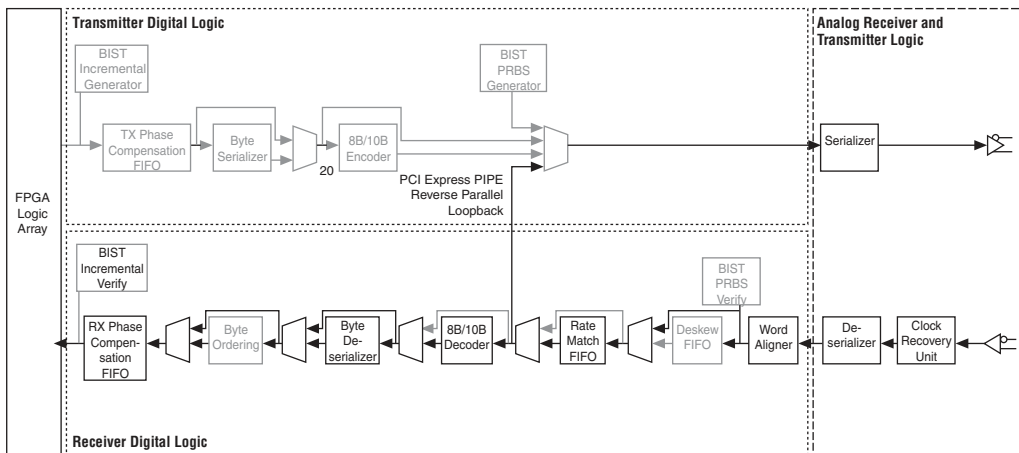


PCI Express PIPE Reverse Parallel Loopback

This loopback mode, available only in PIPE mode, can be dynamically enabled by the tx_detect rxloopback port of the PIPE interface.

Figure 2–28 shows the datapath for this mode.

Figure 2–28. Stratix II GX Block in PCI Express PIPE Reverse Parallel Loopback Mode

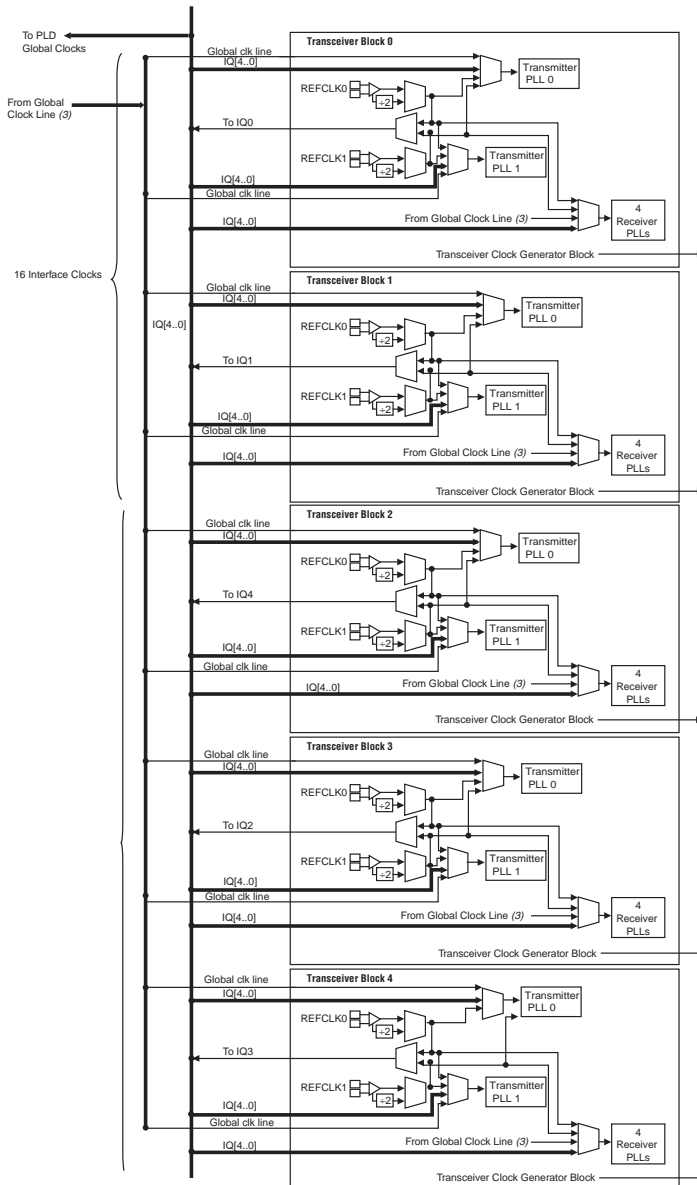


Transceiver Clocking

Each Stratix II GX device transceiver block contains two transmitter PLLs and four receiver PLLs. These PLLs can be driven by either of the two reference clocks per transceiver block. These REFCLK signals can drive all global clocks, transmitter PLL inputs, and all receiver PLL inputs. Subsequently, the transmitter PLL output can only drive global clock lines and the receiver PLL reference clock port. Only one of the two reference clocks in a quad can drive the Inter Quad (I/Q) lines to clock the PLLs in the other quads.

Figure 2-29 shows the inter-transceiver line connections as well as the global clock connections for the EP2SGX130 device.

Figure 2–29. EP2SGX130 Device Inter-Transceiver and Global Clock Connections

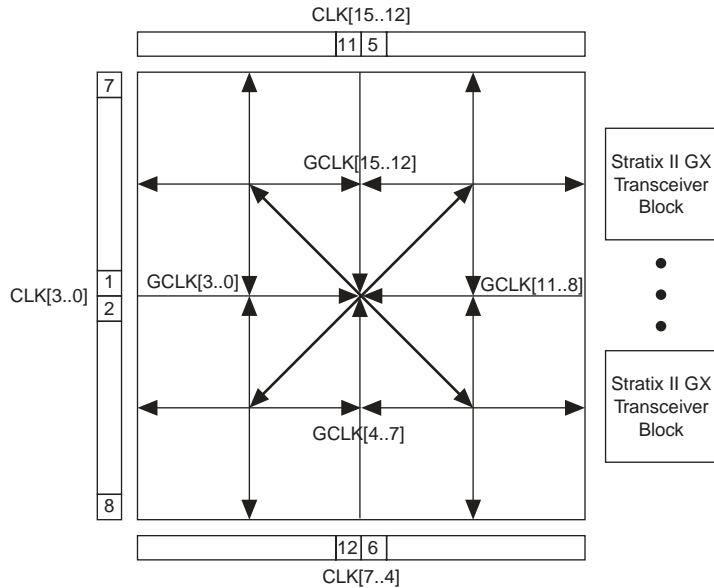


Notes to Figure 2–29:

- (1) There are two transmitter PLLs in each transceiver block.
- (2) There are four receiver PLLs in each transceiver block.
- (3) The Global Clock line must be driven by an input pin.

The receiver PLL can also drive the regional clocks and regional routing adjacent to the associated transceiver block. [Figure 2–30](#) shows which global clock resource can be used by the recovered clock. [Figure 2–31](#) shows which regional clock resource can be used by the recovered clock.

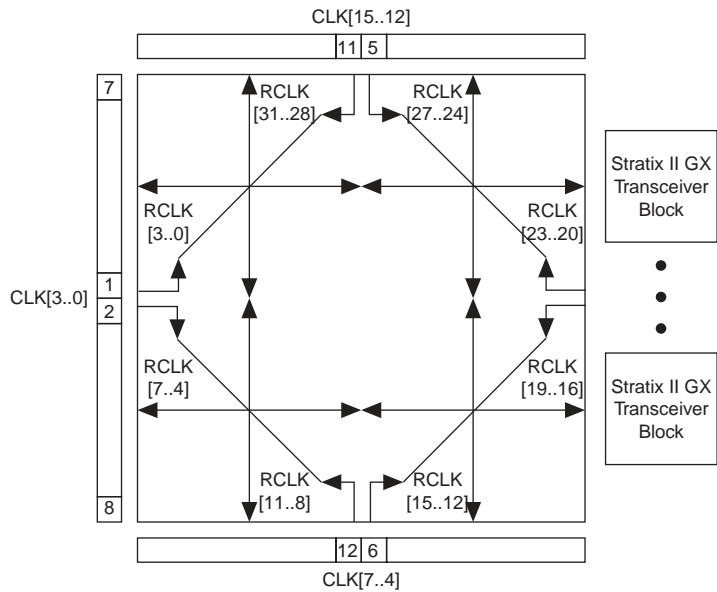
Figure 2–30. Stratix II GX Receiver PLL Recovered Clock to Global Clock Connection *Notes (1), (2)*



Notes to [Figure 2–30](#):

- (1) CLK# pins are clock pins and their associated number. These are pins for global and regional clocks.
- (2) GCLK# pins are global clock pins.

Figure 2–31. Stratix II GX Receiver PLL Recovered Clock to Regional Clock Connection Notes (1), (2)



Notes to Figure 2–31:

- (1) CLK# pins are clock pins and their associated number. These are pins for global and local clocks.
- (2) RCLK# pins are regional clock pins.

Table 2–11 summarizes the possible clocking connections for the transceivers.

| Source | Destination | | | | |
|---|-----------------|--------------|--------------|----------------|-------------------------|
| | Transmitter PLL | Receiver PLL | Global Clock | Regional Clock | Inter-Transceiver Lines |
| REFCLK [1..0] | ✓ | ✓ | ✓ | ✓ | ✓ |
| Transmitter PLL | | | ✓ | ✓ | |
| Receiver PLL | | | ✓ | ✓ | |
| Global clock (driven from an input pin) | ✓ | ✓ | | | |
| Inter-transceiver lines | ✓ | ✓ | | | |

Clock Resource for PLD-Transceiver Interface

For the regional or global clock network to route into the transceiver, a local route input output (LRIO) channel is required. Each LRIO clock region has up to eight clock paths and each transceiver block has a maximum of eight clock paths for connecting with LRIO clocks. These resources are limited and determine the number of clocks that can be used between the PLD and transceiver blocks. Table 2–12 shows the number of LRIO resources available for Stratix II GX devices with different numbers of transceiver blocks.

Tables 2–12 through 2–15 show the connection of the LRIO clock resource to the transceiver block.

| Region | Clock Resource | | Transceiver | |
|-------------------------|----------------|----------------|------------------------|------------------------|
| | Global Clock | Regional Clock | Bank 13 8 Clock I/O | Bank 14 8 Clock I/O |
| Region0 8 LRIO clock | ✓ | RCLK 20-27 | ✓ | |
| Region1 8 LRIO clock | ✓ | RCLK 12-19 | | ✓ |

Table 2–13. Available Clocking Connections for Transceivers in 2SGX60E

| Region | Clock Resource | | Transceiver | | |
|-------------------------|----------------|----------------|------------------------|------------------------|------------------------|
| | Global Clock | Regional Clock | Bank 13 8 Clock I/O | Bank 14 8 Clock I/O | Bank 15 8 Clock I/O |
| Region0 8 LRIO clock | ✓ | RCLK 20-27 | ✓ | | |
| Region1 8 LRIO clock | ✓ | RCLK 20-27 | ✓ | ✓ | |
| Region2 8 LRIO clock | ✓ | RCLK 12-19 | | ✓ | ✓ |
| Region3 8 LRIO clock | ✓ | RCLK 12-19 | | | ✓ |

Table 2–14. Available Clocking Connections for Transceivers in 2SGX90F

| Region | Clock Resource | | Transceiver | | | |
|-------------------------|----------------|----------------|------------------------|------------------------|------------------------|------------------------|
| | Global Clock | Regional Clock | Bank 13 8 Clock I/O | Bank 14 8 Clock I/O | Bank 15 8 clock I/O | Bank 16 8 Clock I/O |
| Region0 8 LRIO clock | ✓ | RCLK 20-27 | ✓ | | | |
| Region1 8 LRIO clock | ✓ | RCLK 20-27 | | ✓ | | |
| Region2 8 LRIO clock | ✓ | RCLK 12-19 | | | ✓ | |
| Region3 8 LRIO clock | ✓ | RCLK 12-19 | | | | ✓ |

Table 2–15. Available Clocking Connections for Transceivers in 2SGX130G

| Region | Clock Resource | | Transceiver | | | | |
|-------------------------|----------------|----------------|------------------------|------------------------|------------------------|------------------------|------------------------|
| | Global Clock | Regional Clock | Bank 13 8 Clock I/O | Bank 14 8 Clock I/O | Bank 15 8 clock I/O | Bank 16 8 Clock I/O | Bank 17 8 Clock I/O |
| Region0 8 LRIO clock | ✓ | RCLK 20-27 | ✓ | | | | |
| Region1 8 LRIO clock | ✓ | RCLK 20-27 | | ✓ | | | |
| Region2 8 LRIO clock | ✓ | RCLK 12-19 | | | ✓ | ✓ | |
| Region3 8 LRIO clock | ✓ | RCLK 12-19 | | | | ✓ | ✓ |

Other Transceiver Features

Other important features of the Stratix II GX transceivers are the power down and reset capabilities, external voltage reference and bias circuitry, and hot swapping.

Calibration Block

The Stratix II GX device uses the calibration block to calibrate the on-chip termination for the PLLs and their associated output buffers and the terminating resistors on the transceivers. The calibration block counters the effects of process, voltage, and temperature (PVT). The calibration block references a derived voltage across an external reference resistor to calibrate the on-chip termination resistors on the Stratix II GX device. The calibration block can be powered down. However, powering down the calibration block during operations may yield transmit and receive data errors.

Dynamic Reconfiguration

This feature allows you to dynamically reconfigure the PMA portion and the channel parameters, such as data rate and functional mode, of the Stratix II GX transceiver. The PMA reconfiguration allows you to quickly optimize the settings for the transceiver's PMA to achieve the intended bit error rate (BER).

The dynamic reconfiguration block can dynamically reconfigure the following PMA settings:

- Pre-emphasis settings
- Equalizer and DC gain settings
- Voltage Output Differential (V_{OD}) settings

The channel reconfiguration allows you to dynamically modify the data rate, local dividers, and the functional mode of the transceiver channel.



Refer to the *Stratix II GX Device Handbook, volume 2*, for more information.

The dynamic reconfiguration block requires an input clock between 2.5 MHz and 50 MHz. The clock for the dynamic reconfiguration block is derived from a high-speed clock and divided down using a counter.

Individual Power Down and Reset for the Transmitter and Receiver

Stratix II GX transceivers offer a power saving advantage with their ability to shut off functions that are not needed. The device can individually reset the receiver and transmitter blocks and the PLLs. The Stratix II GX device can either globally or individually power down and reset the transceiver. [Table 2-16](#) shows the connectivity between the reset signals and the Stratix II GX transceiver blocks. These reset signals can be controlled from the FPGA or pins.

Table 2–16. Reset Signal Map to Stratix II GX Blocks

| Reset Signal | Transmitter Phase Compensation FIFO Module/ Byte Serializer | Transmitter 8B/10B Encoder | Transmitter Serializer | Transmitter Analog Circuits | Transmitter PLL | Transmitter XAUI State Machine | BIST Generators | Receiver Deserializer | Receiver Word Aligner | Receiver Deskew FIFO Module | Receiver Rate Matcher | Receiver 8B/10B Decoder | Receiver Phase Comp FIFO Module/ Byte Deserializer | Receiver PLL / CRU | Receiver XAUI State Machine | BIST Verifiers | Receiver Analog Circuits |
|-----------------|---|----------------------------|------------------------|-----------------------------|-----------------|--------------------------------|-----------------|-----------------------|-----------------------|-----------------------------|-----------------------|-------------------------|--|--------------------|-----------------------------|----------------|--------------------------|
| rx_digitalreset | | | | | | | | ✓ | ✓ | ✓ | ✓ | ✓ | | | ✓ | ✓ | |
| rx_analogreset | | | | | | | | ✓ | | | | | | ✓ | | | ✓ |
| tx_digitalreset | ✓ | ✓ | | | | ✓ | ✓ | | | | | | | | | | |
| gxb_powerdown | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| gxb_enable | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

Voltage Reference Capabilities

Stratix II GX transceivers provide voltage reference and bias circuitry. To set up internal bias for controlling the transmitter output driver voltage swings, as well as to provide voltage and current biasing for other analog circuitry, the device uses an internal bandgap voltage reference of 0.7 V. An external 2-K Ω resistor connected to ground generates a constant bias current (independent of power supply drift, process changes, or temperature variation). An on-chip resistor generates a tracking current that tracks on-chip resistor variation. These currents are mirrored and distributed to the analog circuitry in each channel.



For more information, refer to the *DC and Switching Characteristics* chapter in volume 1 of the *Stratix II GX Handbook*.

Applications and Protocols Supported with Stratix II GX Devices

Each Stratix II GX transceiver block is designed to operate at any serial bit rate from 600 Mbps to 6.375 Gbps per channel. The wide data rate range allows Stratix II GX transceivers to support a wide variety of standards and protocols, such as PCI Express, GIGE, SONET/SDH, SDI, OIF-CEI, and XAUI. Stratix II GX devices are ideal for many high-speed communication applications, such as high-speed backplanes, chip-to-chip bridges, and high-speed serial communications links.

Example Applications Support for Stratix II GX

Stratix II GX devices can be used for many applications, including:

- Traffic management with various levels of quality of service (QoS) and integrated serial backplane interconnect
- Multi-port single-protocol switching (for example, PCI Express, GIGE, XAUI switch, or SONET/SDH)

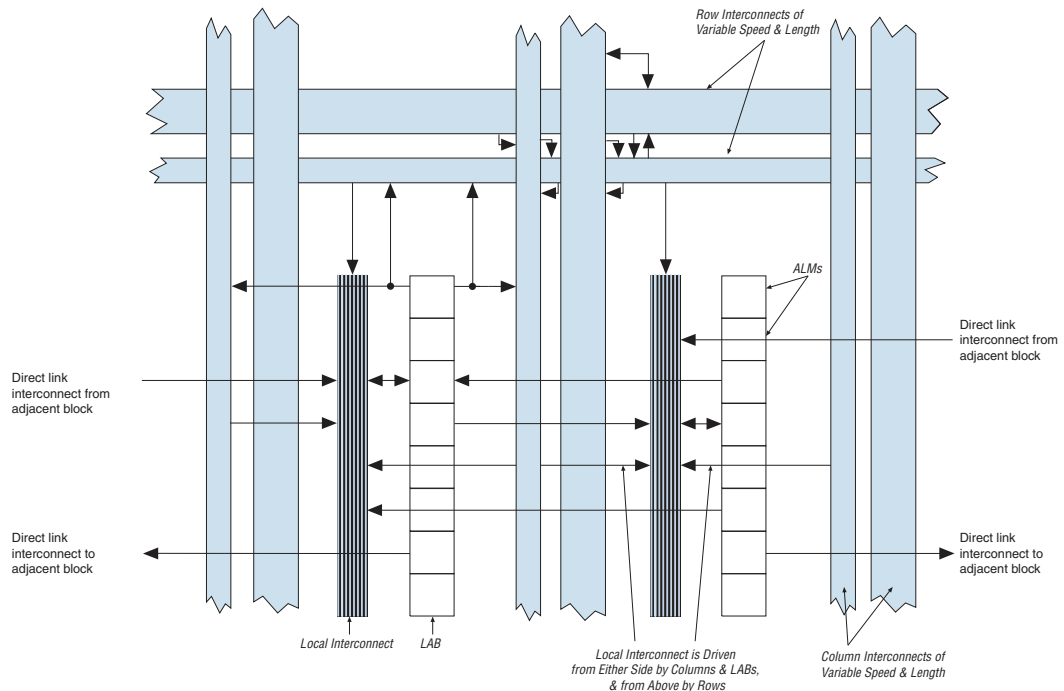
Logic Array Blocks

Each logic array block (LAB) consists of eight adaptive logic modules (ALMs), carry chains, shared arithmetic chains, LAB control signals, local interconnects, and register chain connection lines. The local interconnect transfers signals between ALMs in the same LAB. Register chain connections transfer the output of an ALM register to the adjacent ALM register in a LAB. The Quartus II Compiler places associated logic in a LAB or adjacent LABs, allowing the use of local, shared arithmetic chain, and register chain connections for performance and area efficiency.

Table 2–17 shows Stratix II GX device resources. Figure 2–32 shows the Stratix II GX LAB structure.

| Device | M512 RAM Columns/Blocks | M4K RAM Columns/Blocks | M-RAM Blocks | DSP Block Columns/Blocks | LAB Columns | LAB Rows |
|---------------|------------------------------------|-----------------------------------|-------------------------|-------------------------------------|------------------------|-----------------|
| EP2SGX30 | 6/202 | 4/144 | 1 | 2/16 | 49 | 36 |
| EP2SGX60 | 7/329 | 5/255 | 2 | 3/36 | 62 | 51 |
| EP2SGX90 | 8/488 | 6/408 | 4 | 3/48 | 71 | 68 |
| EP2SGX130 | 9/699 | 7/609 | 6 | 3/63 | 81 | 87 |

Figure 2–32. Stratix II GX LAB Structure

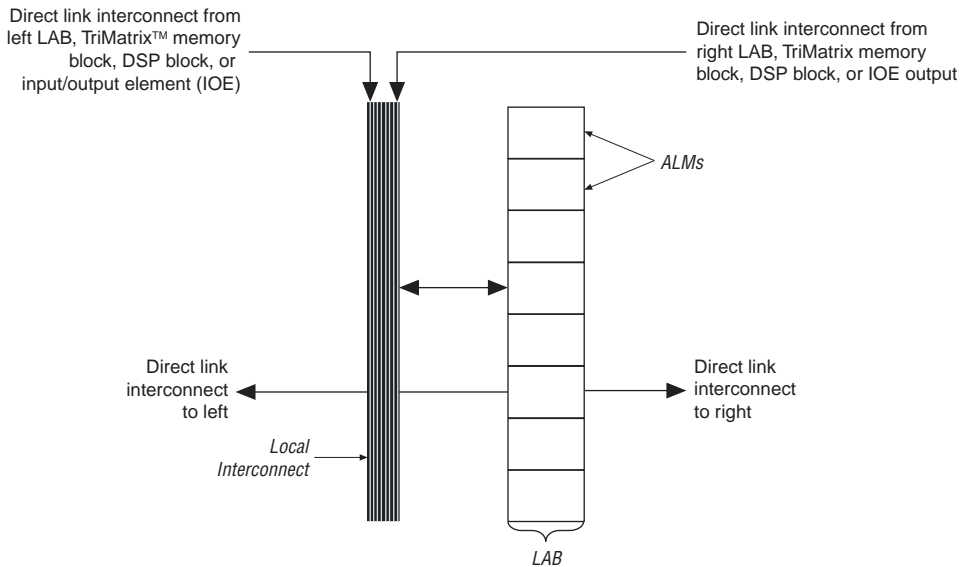


LAB Interconnects

The LAB local interconnect can drive all eight ALMs in the same LAB. It is driven by column and row interconnects and ALM outputs in the same LAB. Neighboring LABs, M512 RAM blocks, M4K RAM blocks, M-RAM blocks, or digital signal processing (DSP) blocks from the left and right can also drive a LAB's local interconnect through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each ALM can drive 24 ALMs through fast local and direct link interconnects.

Figure 2–33 shows the direct link connection.

Figure 2–33. Direct Link Connection



LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its ALMs. The control signals include three clocks, three clock enables, two asynchronous clears, synchronous clear, asynchronous preset/load, and synchronous load control signals, providing a maximum of 11 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

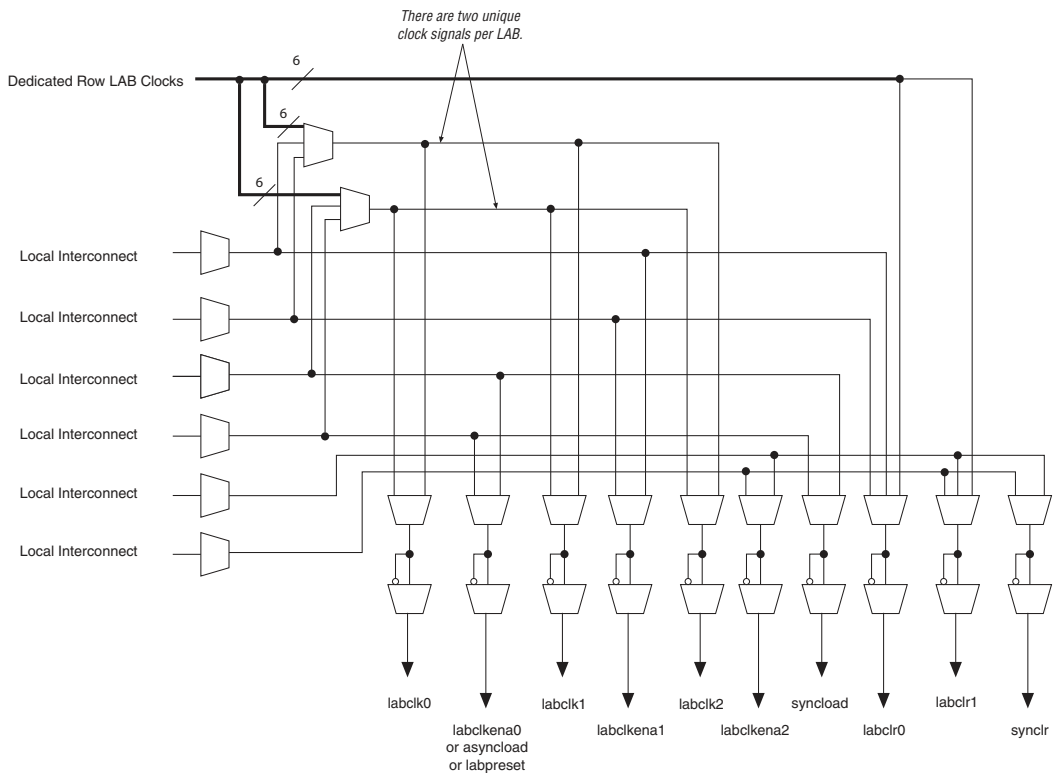
Each LAB can use three clocks and three clock enable signals. However, there can only be up to two unique clocks per LAB, as shown in the LAB control signal generation circuit in Figure 2–34. Each LAB’s clock and clock enable signals are linked. For example, any ALM in a particular LAB using the `labclk1` signal also uses `labckena1`. If the LAB uses both the rising and falling edges of a clock, it also uses two LAB-wide clock signals. De-asserting the clock enable signal turns off the corresponding LAB-wide clock. Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. The asynchronous

load acts as a preset when the asynchronous load data input is tied high. When the asynchronous load/preset signal is used, the `labclkena0` signal is no longer available.

The LAB row clocks [5..0] and LAB local interconnect generate the LAB-wide control signals. The MultiTrack™ interconnects have inherently low skew. This low skew allows the MultiTrack interconnects to distribute clock and control signals in addition to data.

Figure 2–34 shows the LAB control signal generation circuit.

Figure 2–34. LAB-Wide Control Signals



Adaptive Logic Modules

The basic building block of logic in the Stratix II GX architecture is the ALM. The ALM provides advanced features with efficient logic utilization. Each ALM contains a variety of look-up table (LUT)-based resources that can be divided between two adaptive LUTs (ALUTs). With up to eight inputs to the two ALUTs, one ALM can implement various combinations of two functions. This adaptability allows the ALM to be completely backward-compatible with four-input LUT architectures. One ALM can also implement any function of up to six inputs and certain seven-input functions.

In addition to the adaptive LUT-based resources, each ALM contains two programmable registers, two dedicated full adders, a carry chain, a shared arithmetic chain, and a register chain. Through these dedicated resources, the ALM can efficiently implement various arithmetic functions and shift registers. Each ALM drives all types of interconnects: local, row, column, carry chain, shared arithmetic chain, register chain, and direct link interconnects. Figure 2–35 shows a high-level block diagram of the Stratix II GX ALM while Figure 2–36 shows a detailed view of all the connections in the ALM.

Figure 2–35. High-Level Block Diagram of the Stratix II GX ALM

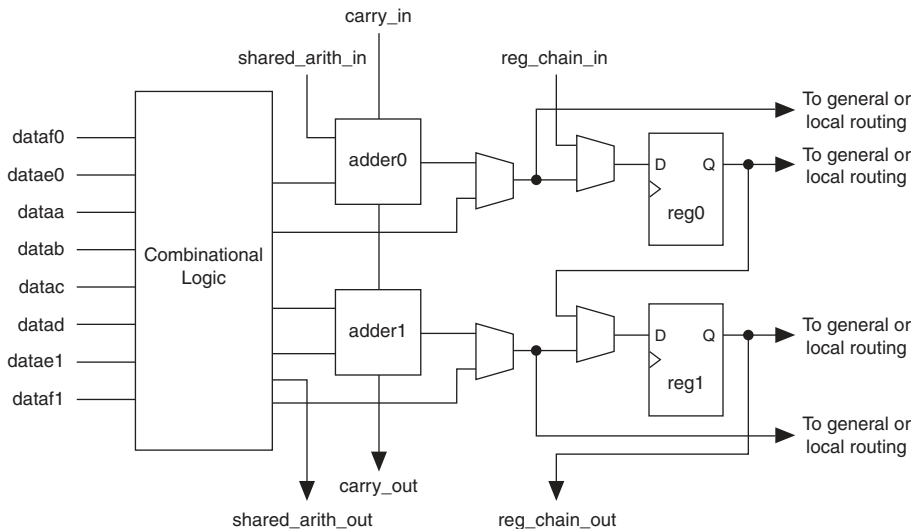
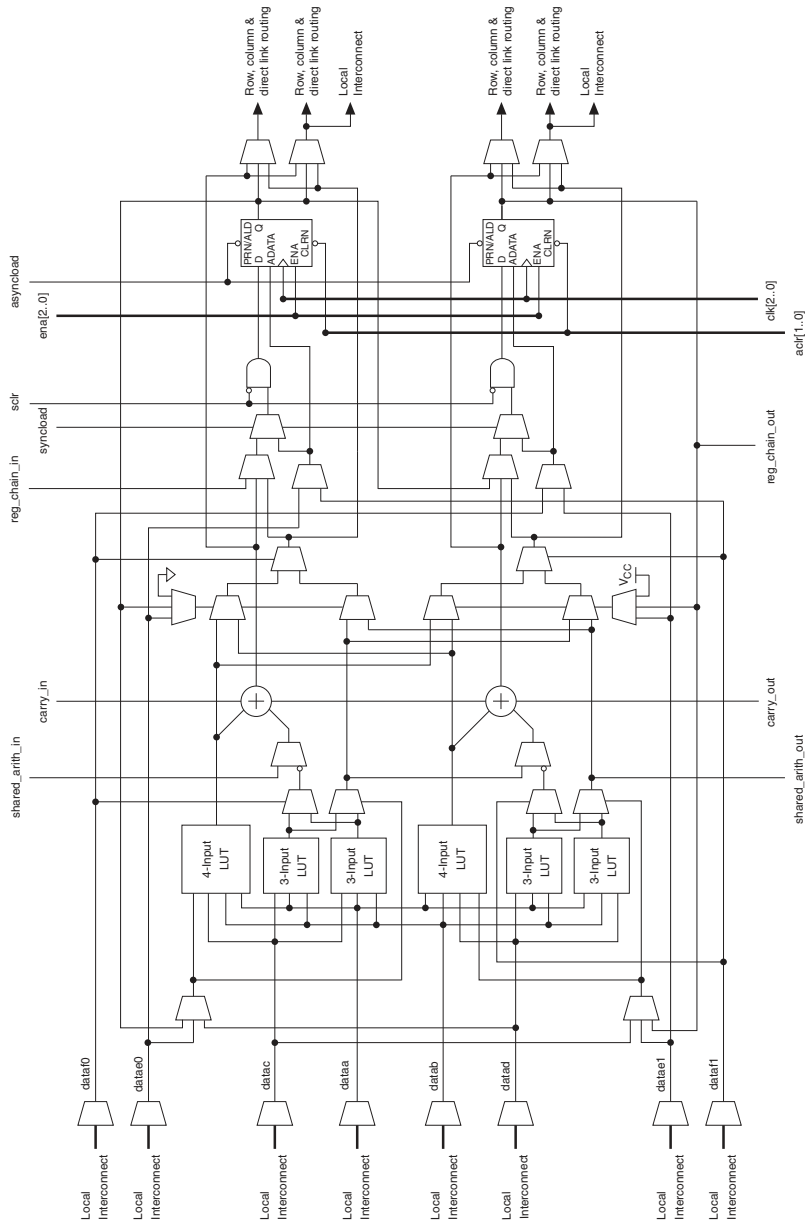


Figure 2–36. Stratix II GX ALM Details



One ALM contains two programmable registers. Each register has data, clock, clock enable, synchronous and asynchronous clear, asynchronous load data, and synchronous and asynchronous load/preset inputs.

Global signals, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable, preset, asynchronous load, and asynchronous load data. The asynchronous load data input comes from the `datae` or `dataf` input of the ALM, which are the same inputs that can be used for register packing. For combinational functions, the register is bypassed and the output of the LUT drives directly to the outputs of the ALM.

Each ALM has two sets of outputs that drive the local, row, and column routing resources. The LUT, adder, or register output can drive these output drivers independently (see [Figure 2–36](#)). For each set of output drivers, two ALM outputs can drive column, row, or direct link routing connections, and one of these ALM outputs can also drive local interconnect resources. This allows the LUT or adder to drive one output while the register drives another output. This feature, called register packing, improves device utilization because the device can use the register and the combinational logic for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same ALM so that the register is packed with its own fan-out LUT. This feature provides another mechanism for improved fitting. The ALM can also drive out registered and unregistered versions of the LUT or adder output.



See the [Stratix II Performance and Logic Efficiency Analysis White Paper](#) for more information on the efficiencies of the Stratix II GX ALM and comparisons with previous architectures.

ALM Operating Modes

The Stratix II GX ALM can operate in one of the following modes:

- Normal mode
- Extended LUT mode
- Arithmetic mode
- Shared arithmetic mode

Each mode uses ALM resources differently. Each mode has 11 available inputs to the ALM (see [Figure 2–35](#))—the eight data inputs from the LAB local interconnect; carry-in from the previous ALM or LAB; the shared arithmetic chain connection from the previous ALM or LAB; and the register chain connection—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock,

asynchronous clear, asynchronous preset/load, synchronous clear, synchronous load, and clock enable control for the register. These LAB wide signals are available in all ALM modes. Refer to “[LAB Control Signals](#)” on page 2–46 for more information on the LAB-wide control signals.

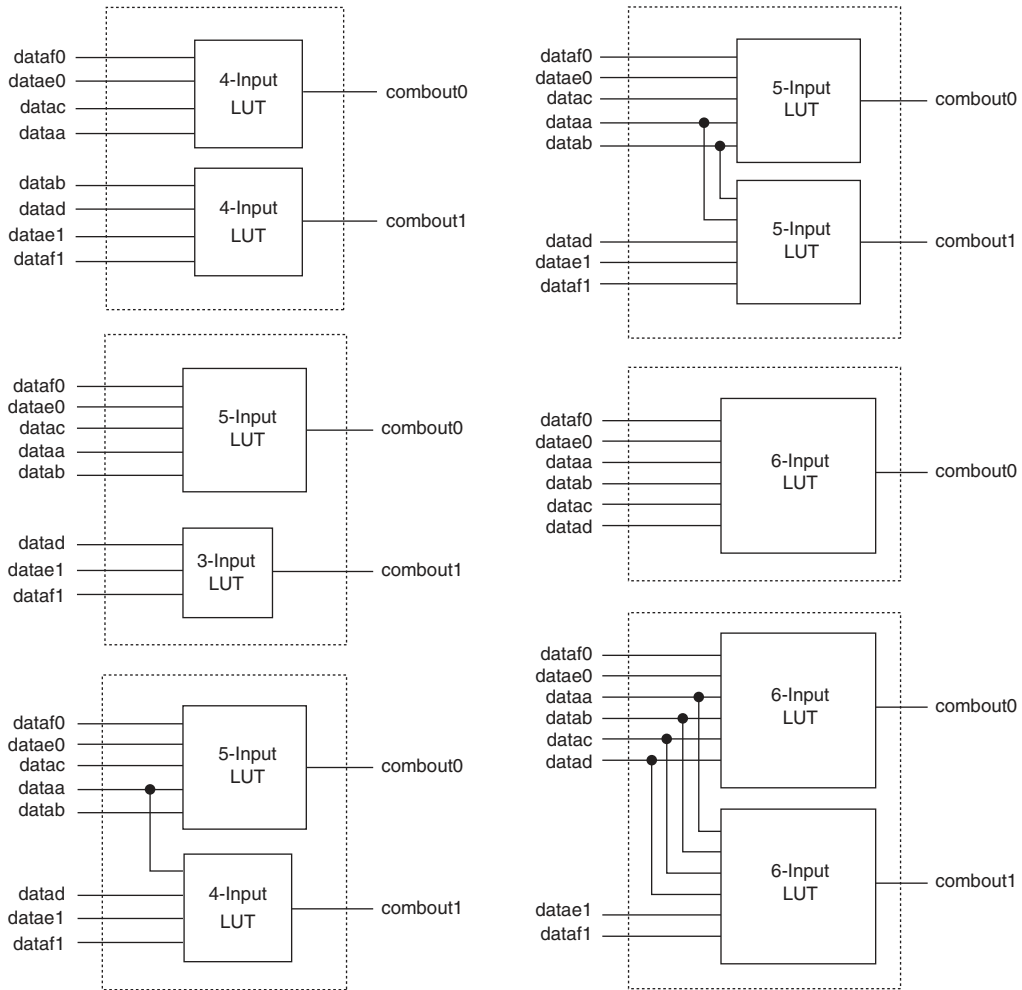
The Quartus II software and supported third-party synthesis tools, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically choose the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions. If required, you can also create special-purpose functions that specify which ALM operating mode to use for optimal performance.

Normal Mode

The normal mode is suitable for general logic applications and combinational functions. In this mode, up to eight data inputs from the LAB local interconnect are inputs to the combinational logic. The normal mode allows two functions to be implemented in one Stratix II GX ALM, or an ALM to implement a single function of up to six inputs. The ALM can support certain combinations of completely independent functions and various combinations of functions which have common inputs.

[Figure 2–37](#) shows the supported LUT combinations in normal mode.

Figure 2–37. ALM in Normal Mode *Note (1)*



Note to Figure 2–37:

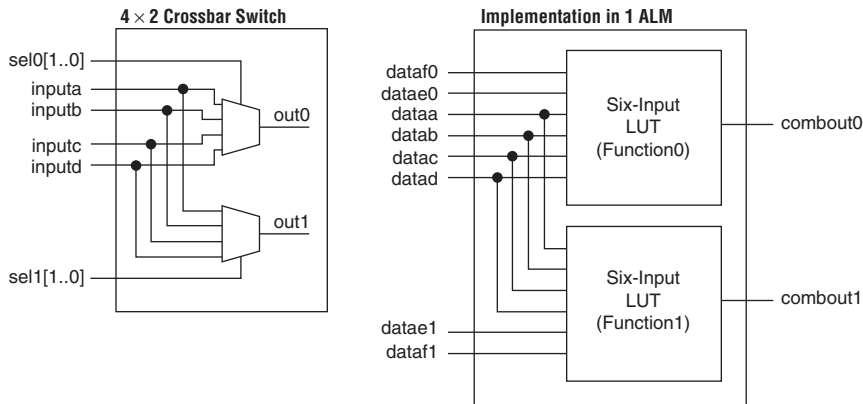
- (1) Combinations of functions with less inputs than those shown are also supported. For example, combinations of functions with the following number of inputs are supported: 4 and 3, 3 and 3, 3 and 2, 5 and 2, etc.

The normal mode provides complete backward compatibility with four-input LUT architectures. Two independent functions of four inputs or less can be implemented in one Stratix II GX ALM. In addition, a five-input function and an independent three-input function can be implemented without sharing inputs.

To pack two five-input functions into one ALM, the functions must have at least two common inputs. The common inputs are `dataaa` and `datab`. The combination of a four-input function with a five-input function requires one common input (either `dataaa` or `datab`).

To implement two six-input functions in one ALM, four inputs must be shared and the combinational function must be the same. For example, a 4×2 crossbar switch (two 4-to-1 multiplexers with common inputs and unique select lines) can be implemented in one ALM, as shown in [Figure 2–38](#). The shared inputs are `dataaa`, `datab`, `dataac`, and `datad`, while the unique select lines are `datae0` and `dataf0` for `function0`, and `datae1` and `dataf1` for `function1`. This crossbar switch consumes four LUTs in a four-input LUT-based architecture.

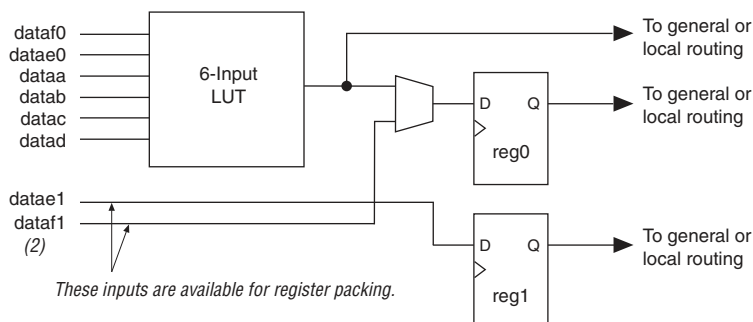
Figure 2–38. 4×2 Crossbar Switch Example



In a sparsely used device, functions that could be placed into one ALM can be implemented in separate ALMs. The Quartus II Compiler spreads a design out to achieve the best possible performance. As a device begins to fill up, the Quartus II software automatically utilizes the full potential of the Stratix II GX ALM. The Quartus II Compiler automatically searches for functions of common inputs or completely independent functions to be placed into one ALM and to make efficient use of the device resources. In addition, you can manually control resource usage by setting location assignments. Any six-input function can be implemented utilizing inputs `dataaa`, `datab`, `dataac`, `datad`, and either `datae0` and `dataf0` or `datae1` and `dataf1`. If `datae0` and `dataf0` are utilized, the output is driven to `register0`, and/or `register0` is bypassed and the data drives out to the interconnect using the top set of output drivers (see [Figure 2–39](#)). If `datae1` and `dataf1` are utilized, the output drives to `register1` and/or bypasses `register1` and drives to the interconnect

using the bottom set of output drivers. The Quartus II Compiler automatically selects the inputs to the LUT. Asynchronous load data for the register comes from the `dataae` or `dataaf` input of the ALM. ALMs in normal mode support register packing.

Figure 2–39. 6-Input Function in Normal Mode Notes (1), (2)

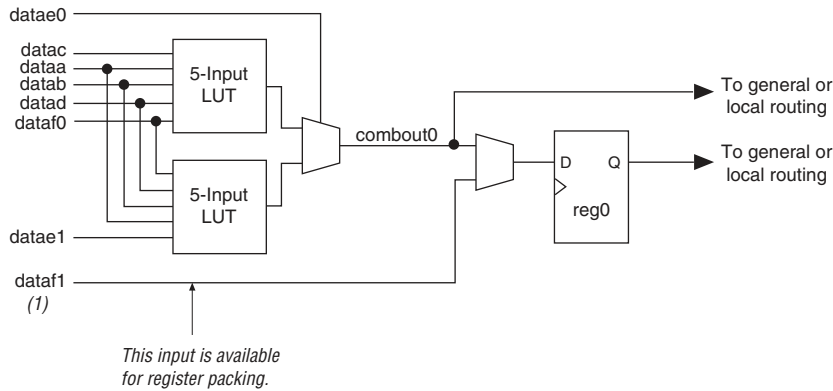


Notes to Figure 2–39:

- (1) If `datae1` and `dataf1` are used as inputs to the six-input function, `datae0` and `dataf0` are available for register packing.
- (2) The `dataf1` input is available for register packing only if the six-input function is unregistered.

Extended LUT Mode

The extended LUT mode is used to implement a specific set of seven-input functions. The set must be a 2-to-1 multiplexer fed by two arbitrary five-input functions sharing four inputs. Figure 2–40 shows the template of supported seven-input functions utilizing extended LUT mode. In this mode, if the seven-input function is unregistered, the unused eighth input is available for register packing. Functions that fit into the template shown in Figure 2–40 occur naturally in designs. These functions often appear in designs as “if-else” statements in Verilog HDL or VHDL code.

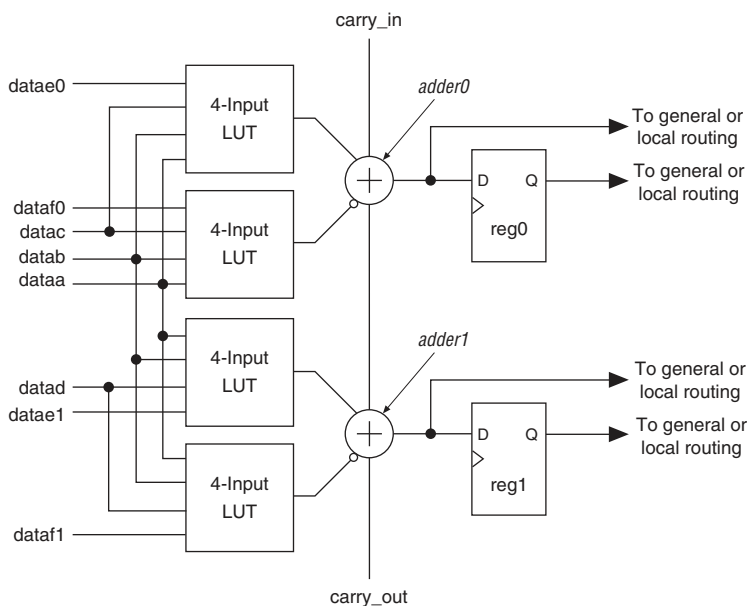
Figure 2–40. Template for Supported Seven-Input Functions in Extended LUT Mode**Note to Figure 2–40:**

- (1) If the seven-input function is un-registered, the unused eighth input is available for register packing. The second register, `reg1`, is not available.

Arithmetic Mode

The arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. An ALM in arithmetic mode uses two sets of two four-input LUTs along with two dedicated full adders. The dedicated adders allow the LUTs to be available to perform pre-adder logic; therefore, each adder can add the output of two four-input functions. The four LUTs share the `dataa` and `datab` inputs. As shown in Figure 2–41, the carry-in signal feeds to `adder0`, and the carry-out from `adder0` feeds to carry-in of `adder1`. The carry-out from `adder1` drives to `adder0` of the next ALM in the LAB. ALMs in arithmetic mode can drive out registered and/or un-registered versions of the adder outputs.

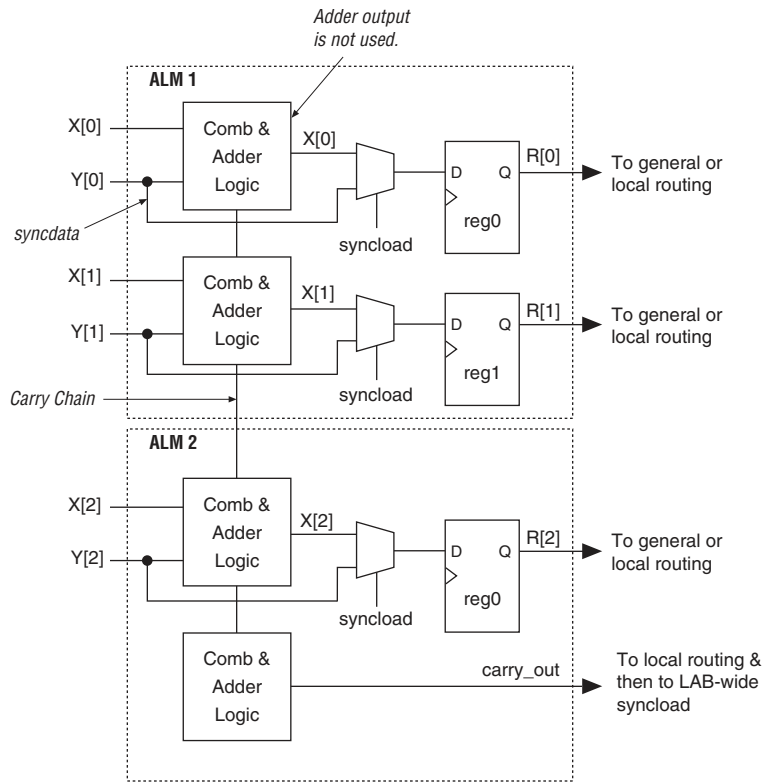
Figure 2-41. ALM in Arithmetic Mode



While operating in arithmetic mode, the ALM can support simultaneous use of the adder's carry output along with combinational logic outputs. In this operation, the adder output is ignored. This usage of the adder with the combinational logic output provides resource savings of up to 50% for functions that can use this ability. An example of such functionality is a conditional operation, such as the one shown in [Figure 2-42](#). The equation for this example is:

$$R = (X < Y) ? Y : X$$

To implement this function, the adder is used to subtract 'Y' from 'X'. If 'X' is less than 'Y', the *carry_out* signal will be '1'. The *carry_out* signal is fed to an adder where it drives out to the LAB local interconnect. It then feeds to the LAB-wide *syncload* signal. When asserted, *syncload* selects the *syncdata* input. In this case, the data 'Y' drives the *syncdata* inputs to the registers. If 'X' is greater than or equal to 'Y', the *syncload* signal is de-asserted and 'X' drives the data port of the registers.

Figure 2–42. Conditional Operation Example

The arithmetic mode also offers clock enable, counter enable, synchronous up and down control, add and subtract control, synchronous clear, synchronous load. The LAB local interconnect data inputs generate the clock enable, counter enable, synchronous up and down and add and subtract control signals. These control signals may be used for the inputs that are shared between the four LUTs in the ALM. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

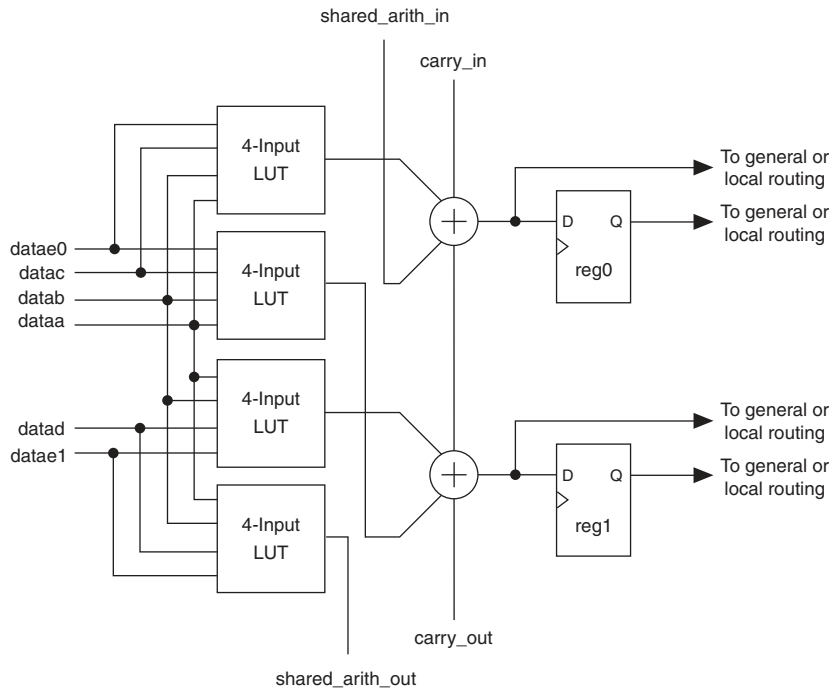
Carry Chain

The carry chain provides a fast carry function between the dedicated adders in arithmetic or shared arithmetic mode. Carry chains can begin in either the first ALM or the fifth ALM in a LAB. The final carry-out signal is routed to an ALM, where it is fed to local, row, or column interconnects.

The Quartus II Compiler automatically creates carry chain logic during compilation, or you can create it manually during design entry. Parameterized functions, such as LPM functions, automatically take advantage of carry chains for the appropriate functions. The Quartus II Compiler creates carry chains longer than 16 (8 ALMs in arithmetic or shared arithmetic mode) by linking LABs together automatically. For enhanced fitting, a long carry chain runs vertically, allowing fast horizontal connections to TriMatrix memory and DSP blocks. A carry chain can continue as far as a full column. To avoid routing congestion in one small area of the device when a high fan-in arithmetic function is implemented, the LAB can support carry chains that only utilize either the top half or the bottom half of the LAB before connecting to the next LAB. The other half of the ALMs in the LAB is available for implementing narrower fan-in functions in normal mode. Carry chains that use the top four ALMs in the first LAB will carry into the top half of the ALMs in the next LAB within the column. Carry chains that use the bottom four ALMs in the first LAB will carry into the bottom half of the ALMs in the next LAB within the column. Every other column of the LABs are top-half bypassable, while the other LAB columns are bottom-half bypassable. Refer to [“MultiTrack Interconnect” on page 2–63](#) for more information on carry chain interconnect.

Shared Arithmetic Mode

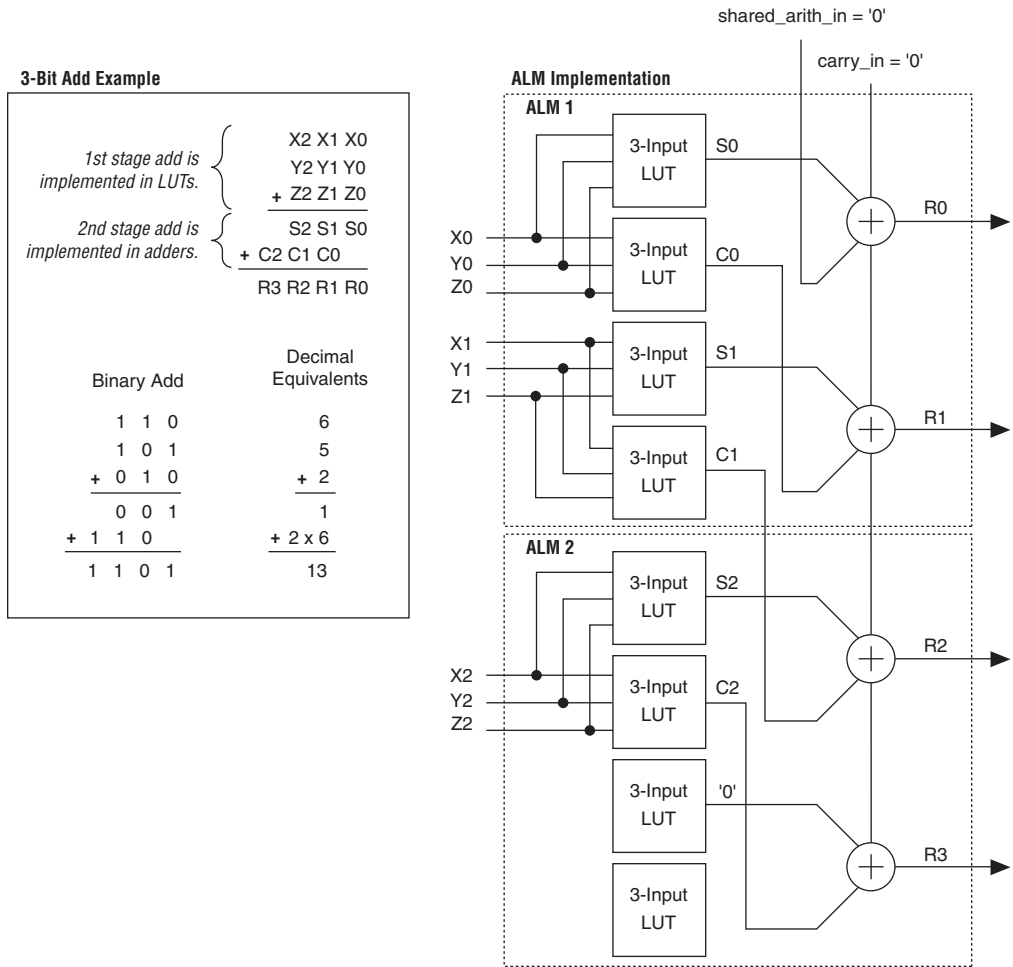
In shared arithmetic mode, the ALM can implement a three-input add. In this mode, the ALM is configured with four 4-input LUTs. Each LUT either computes the sum of three inputs or the carry of three inputs. The output of the carry computation is fed to the next adder (either to `adder1` in the same ALM or to `adder0` of the next ALM in the LAB) using a dedicated connection called the shared arithmetic chain. This shared arithmetic chain can significantly improve the performance of an adder tree by reducing the number of summation stages required to implement an adder tree. [Figure 2–43](#) shows the ALM in shared arithmetic mode.

Figure 2–43. ALM in Shared Arithmetic Mode**Note to Figure 2–43:**

- (1) Inputs dataf0 and dataf1 are available for register packing in shared arithmetic mode.

Adder trees are used in many different applications. For example, the summation of the partial products in a logic-based multiplier can be implemented in a tree structure. Another example is a correlator function that can use a large adder tree to sum filtered data samples in a given time frame to recover or to de-spread data which was transmitted utilizing spread spectrum technology. An example of a three-bit add operation utilizing the shared arithmetic mode is shown in Figure 2–44. The partial sum ($S[2..0]$) and the partial carry ($C[2..0]$) is obtained using the LUTs, while the result ($R[2..0]$) is computed using the dedicated adders.

Figure 2–44. Example of a 3-Bit Add Utilizing Shared Arithmetic Mode



Shared Arithmetic Chain

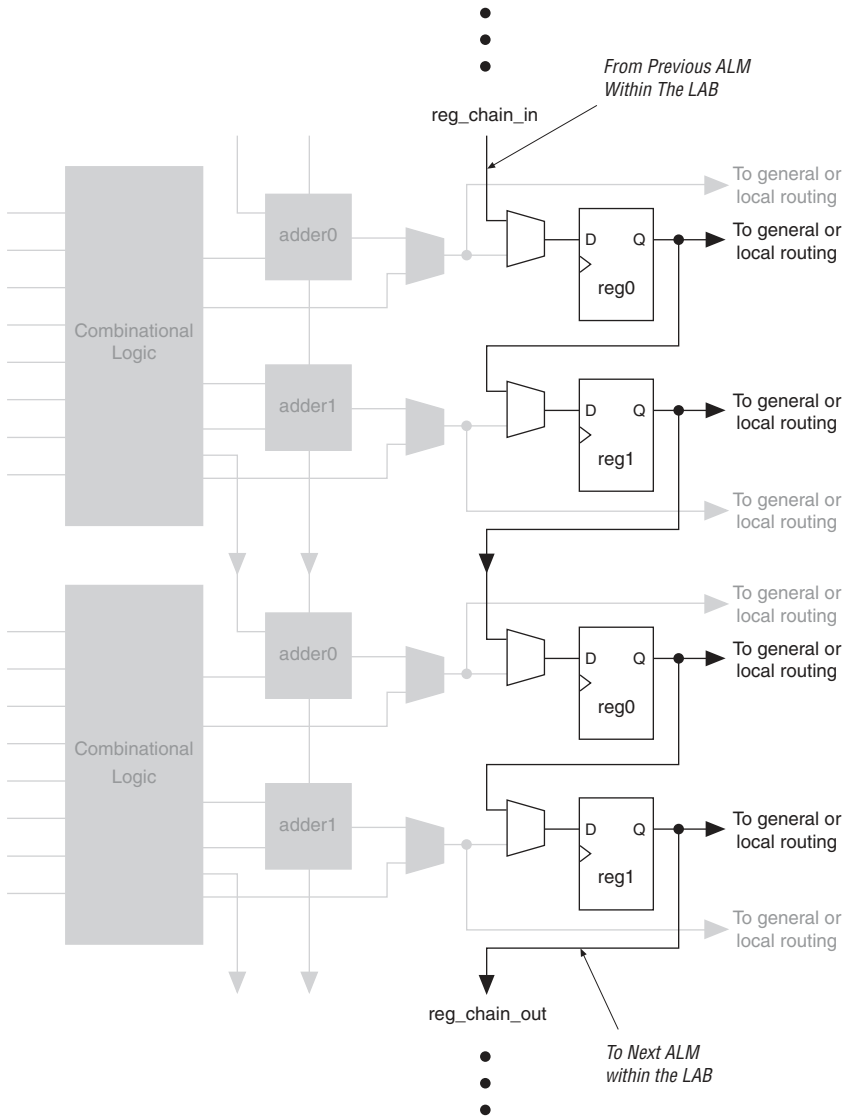
In addition to the dedicated carry chain routing, the shared arithmetic chain available in shared arithmetic mode allows the ALM to implement a three-input add, which significantly reduces the resources necessary to implement large adder trees or correlator functions. The shared arithmetic chains can begin in either the first or fifth ALM in a LAB. The Quartus II Compiler automatically links LABs to create shared arithmetic chains longer than 16 (8 ALMs in arithmetic or shared arithmetic mode). For enhanced fitting, a long shared arithmetic chain runs vertically

allowing fast horizontal connections to TriMatrix memory and DSP blocks. A shared arithmetic chain can continue as far as a full column. Similar to the carry chains, the shared arithmetic chains are also top- or bottom-half bypassable. This capability allows the shared arithmetic chain to cascade through half of the ALMs in a LAB while leaving the other half available for narrower fan-in functionality. Every other LAB column is top-half bypassable, while the other LAB columns are bottom-half bypassable. Refer to [“MultiTrack Interconnect” on page 2-63](#) for more information on shared arithmetic chain interconnect.

Register Chain

In addition to the general routing outputs, the ALMs in a LAB have register chain outputs. The register chain routing allows registers in the same LAB to be cascaded together. The register chain interconnect allows a LAB to use LUTs for a single combinational function and the registers to be used for an unrelated shift register implementation. These resources speed up connections between ALMs while saving local interconnect resources (see [Figure 2-45](#)). The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. See [“MultiTrack Interconnect” on page 2-63](#) for more information about register chain interconnect.

Figure 2–45. Register Chain within a LAB *Note (1)*



Note to Figure 2–45:

(1) The combinational or adder logic can be utilized to implement an unrelated, un-registered function.

Clear and Preset Logic Control

LAB-wide signals control the logic for the register's clear and load/preset signals. The ALM directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. The direct asynchronous preset does not require a NOT gate push-back technique. Stratix II GX devices support simultaneous asynchronous load/preset and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one load/preset signal.

In addition to the clear and load/preset ports, Stratix II GX devices provide a device-wide reset pin (DEV_CLRn) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This device-wide reset overrides all other control signals.

MultiTrack Interconnect

In the Stratix II GX architecture, the MultiTrack interconnect structure with DirectDrive technology provides connections between ALMs, TriMatrix memory, DSP blocks, and device I/O pins. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different lengths and speeds used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement in the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when migrating through different device densities. Dedicated row interconnects route signals to and from LABs, DSP blocks, and TriMatrix memory in the same row.

These row resources include:

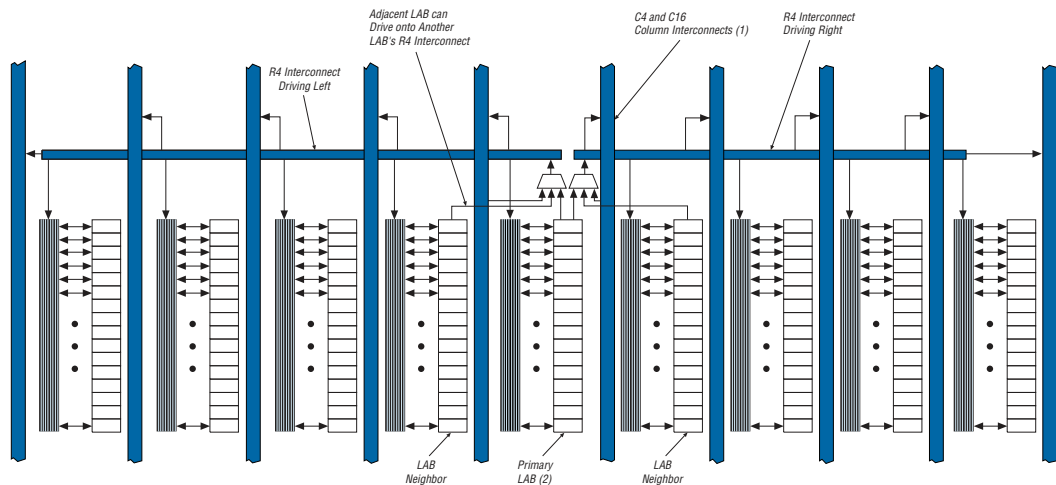
- Direct link interconnects between LABs and adjacent blocks
- R4 interconnects traversing four blocks to the right or left
- R24 row interconnects for high-speed access across the length of the device

The direct link interconnect allows a LAB, DSP block, or TriMatrix memory block to drive into the local interconnect of its left and right neighbors and then back into itself, providing fast communication between adjacent LABs and/or blocks without using row interconnect resources.

The R4 interconnects span four LABs, three LABs and one M512 RAM block, two LABs and one M4K RAM block, or two LABs and one DSP block to the right or left of a source LAB. These resources are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. [Figure 2-46](#) shows R4 interconnect connections from a LAB.

R4 interconnects can drive and be driven by DSP blocks and RAM blocks and row IOEs. For LAB interfacing, a primary LAB or LAB neighbor can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive onto the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive onto the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. R4 interconnects can also drive C4 and C16 interconnects for connections from one row to another. Additionally, R4 interconnects can drive R24 interconnects.

Figure 2-46. R4 Interconnect Connections *Notes (1), (2), (3)*



Notes to [Figure 2-46](#):

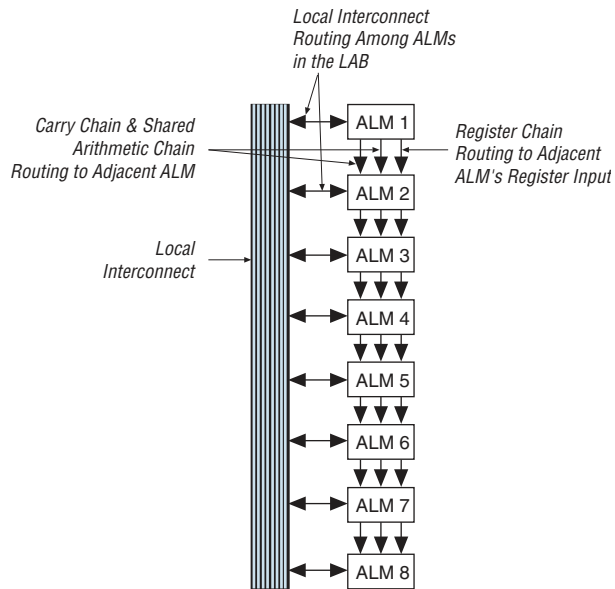
- (1) C4 and C16 interconnects can drive R4 interconnects.
- (2) This pattern is repeated for every LAB in the LAB row.
- (3) The LABs in [Figure 2-46](#) show the 16 possible logical outputs per LAB.

R24 row interconnects span 24 LABs and provide the fastest resource for long row connections between LABs, TriMatrix memory, DSP blocks, and Row IOEs. The R24 row interconnects can cross M-RAM blocks. R24 row interconnects drive to other row or column interconnects at every fourth LAB and do not drive directly to LAB local interconnects. R24 row interconnects drive LAB local interconnects via R4 and C4 interconnects. R24 interconnects can drive R24, R4, C16, and C4 interconnects. The column interconnect operates similarly to the row interconnect and vertically routes signals to and from LABs, TriMatrix memory, DSP blocks, and IOEs. Each column of LABs is served by a dedicated column interconnect.

These column resources include:

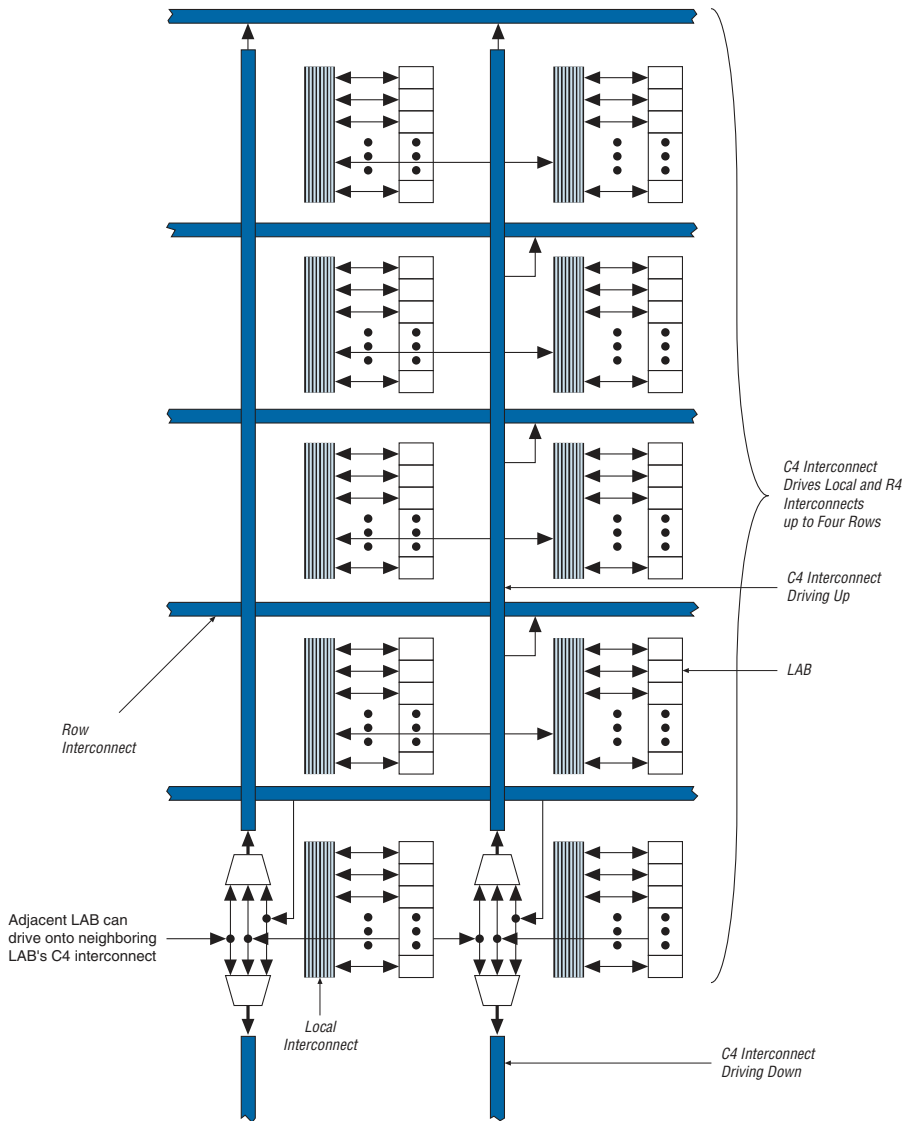
- Shared arithmetic chain interconnects in a LAB
- Carry chain interconnects in a LAB and from LAB to LAB
- Register chain interconnects in a LAB
- C4 interconnects traversing a distance of four blocks in an up and down direction
- C16 column interconnects for high-speed vertical routing through the device

Stratix II GX devices include an enhanced interconnect structure in LABs for routing shared arithmetic chains and carry chains for efficient arithmetic functions. The register chain connection allows the register output of one ALM to connect directly to the register input of the next ALM in the LAB for fast shift registers. These ALM-to-ALM connections bypass the local interconnect. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. [Figure 2-47](#) shows the shared arithmetic chain, carry chain, and register chain interconnects.

Figure 2–47. Shared Arithmetic Chain, Carry Chain and Register Chain Interconnects

The C4 interconnects span four LABs, M512, or M4K blocks up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. [Figure 2–48](#) shows the C4 interconnect connections from a LAB in a column. The C4 interconnects can drive and be driven by all types of architecture blocks, including DSP blocks, TriMatrix memory blocks, and column and row IOEs. For LAB interconnection, a primary LAB or its LAB neighbor can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

Figure 2-48. C4 Interconnect Connections *Note (1)*



Note to Figure 2-48:

- (1) Each C4 interconnect can drive either up or down four rows.

C16 column interconnects span a length of 16 LABs and provide the fastest resource for long column connections between LABs, TriMatrix memory blocks, DSP blocks, and IOEs. C16 interconnects can cross M-RAM blocks and also drive to row and column interconnects at every fourth LAB. C16 interconnects drive LAB local interconnects via C4 and R4 interconnects and do not drive LAB local interconnects directly. All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (that is, TriMatrix memory and DSP blocks) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB. All blocks are fed by the row LAB clocks, `labclk[5..0]`.

Table 2–18 shows the Stratix II GX device’s routing scheme.

Table 2–18. Stratix II GX Device Routing Scheme (Part 1 of 2)

| Source | Destination | | | | | | | | | | | | | | | |
|--------------------------|-------------------------|-------------|----------------|--------------------|--------------------------|-----------------|------------------|-----------------|------------------|-----|----------------|---------------|-------------|------------|------------|---------|
| | Shared Arithmetic Chain | Carry Chain | Register Chain | Local Interconnect | Direct Link Interconnect | R4 Interconnect | R24 Interconnect | C4 Interconnect | C16 Interconnect | ALM | M512 RAM Block | M4K RAM Block | M-RAM Block | DSP Blocks | Column IOE | Row IOE |
| Shared arithmetic chain | | | | | | | | | | ✓ | | | | | | |
| Carry chain | | | | | | | | | | ✓ | | | | | | |
| Register chain | | | | | | | | | | ✓ | | | | | | |
| Local interconnect | | | | | | | | | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Direct link interconnect | | | | ✓ | | | | | | | | | | | | |
| R4 interconnect | | | | ✓ | | ✓ | ✓ | ✓ | ✓ | | | | | | | |
| R24 interconnect | | | | | | ✓ | ✓ | ✓ | ✓ | | | | | | | |
| C4 interconnect | | | | ✓ | | ✓ | | ✓ | | | | | | | | |
| C16 interconnect | | | | | | ✓ | ✓ | ✓ | ✓ | | | | | | | |
| ALM | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ | | | | | | | | |
| M512 RAM block | | | | ✓ | ✓ | ✓ | | ✓ | | | | | | | | |
| M4K RAM block | | | | ✓ | ✓ | ✓ | | ✓ | | | | | | | | |
| M-RAM block | | | | | ✓ | ✓ | ✓ | ✓ | | | | | | | | |
| DSP blocks | | | | | ✓ | ✓ | | ✓ | | | | | | | | |

Table 2–18. Stratix II GX Device Routing Scheme (Part 2 of 2)

| Source | Destination | | | | | | | | | | | | | | | | |
|------------|-------------------------|-------------|----------------|--------------------|--------------------------|-----------------|------------------|-----------------|------------------|-----|----------------|---------------|-------------|------------|------------|---------|--|
| | Shared Arithmetic Chain | Carry Chain | Register Chain | Local Interconnect | Direct Link Interconnect | R4 Interconnect | R24 Interconnect | C4 Interconnect | C16 Interconnect | ALM | M512 RAM Block | M4K RAM Block | M-RAM Block | DSP Blocks | Column IOE | Row IOE | |
| Column IOE | | | | | ✓ | | | ✓ | ✓ | | | | | | | | |
| Row IOE | | | | | ✓ | ✓ | ✓ | ✓ | | | | | | | | | |

TriMatrix Memory

TriMatrix memory consists of three types of RAM blocks: M512, M4K, and M-RAM. Although these memory blocks are different, they can all implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and FIFO buffers. Table 2–19 shows the size and features of the different RAM blocks.

Table 2–19. TriMatrix Memory Features (Part 1 of 2)

| Memory Feature | M512 RAM Block (32 × 18 Bits) | M4K RAM Block (128 × 36 Bits) | M-RAM Block (4K × 144 Bits) |
|------------------------------|----------------------------------|----------------------------------|--------------------------------|
| Maximum performance | 500 MHz | 550 MHz | 420 MHz |
| True dual-port memory | | ✓ | ✓ |
| Simple dual-port memory | ✓ | ✓ | ✓ |
| Single-port memory | ✓ | ✓ | ✓ |
| Shift register | ✓ | ✓ | |
| ROM | ✓ | ✓ | (1) |
| FIFO buffer | ✓ | ✓ | ✓ |
| Pack mode | | ✓ | ✓ |
| Byte enable | ✓ | ✓ | ✓ |
| Address clock enable | | ✓ | ✓ |
| Parity bits | ✓ | ✓ | ✓ |
| Mixed clock mode | ✓ | ✓ | ✓ |
| Memory initialization (.mif) | ✓ | ✓ | |

Table 2–19. TriMatrix Memory Features (Part 2 of 2)

| Memory Feature | M512 RAM Block (32 × 18 Bits) | M4K RAM Block (128 × 36 Bits) | M-RAM Block (4K × 144 Bits) |
|---|---|--|--|
| Simple dual-port memory mixed width support | ✓ | ✓ | ✓ |
| True dual-port memory mixed width support | | ✓ | ✓ |
| Power-up conditions | Outputs cleared | Outputs cleared | Outputs unknown |
| Register clears | Output registers | Output registers | Output registers |
| Mixed-port read-during-write | Unknown output/old data | Unknown output/old data | Unknown output |
| Configurations | 512 × 1 256 × 2 128 × 4 64 × 8 64 × 9 32 × 16 32 × 18 | 4K × 1 2K × 2 1K × 4 512 × 8 512 × 9 256 × 16 256 × 18 128 × 32 128 × 36 | 64K × 8 64K × 9 32K × 16 32K × 18 16K × 32 16K × 36 8K × 64 8K × 72 4K × 128 4K × 144 |

Note to Table 2–19:

- (1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

TriMatrix memory provides three different memory sizes for efficient application support. The Quartus II software automatically partitions the user-defined memory into the embedded memory blocks using the most efficient size combinations. You can also manually assign the memory to a specific block size or a mixture of block sizes.

M512 RAM Block

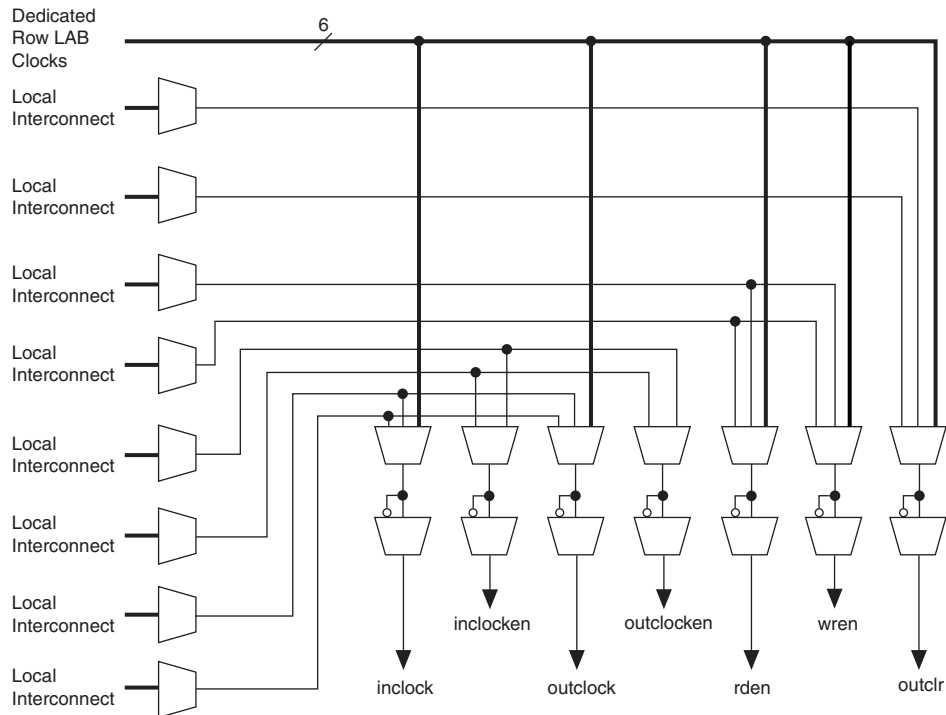
The M512 RAM block is a simple dual-port memory block and is useful for implementing small FIFO buffers, DSP, and clock domain transfer applications. Each block contains 576 RAM bits (including parity bits). M512 RAM blocks can be configured in the following modes:

- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

When configured as RAM or ROM, you can use an initialization file to pre-load the memory contents.

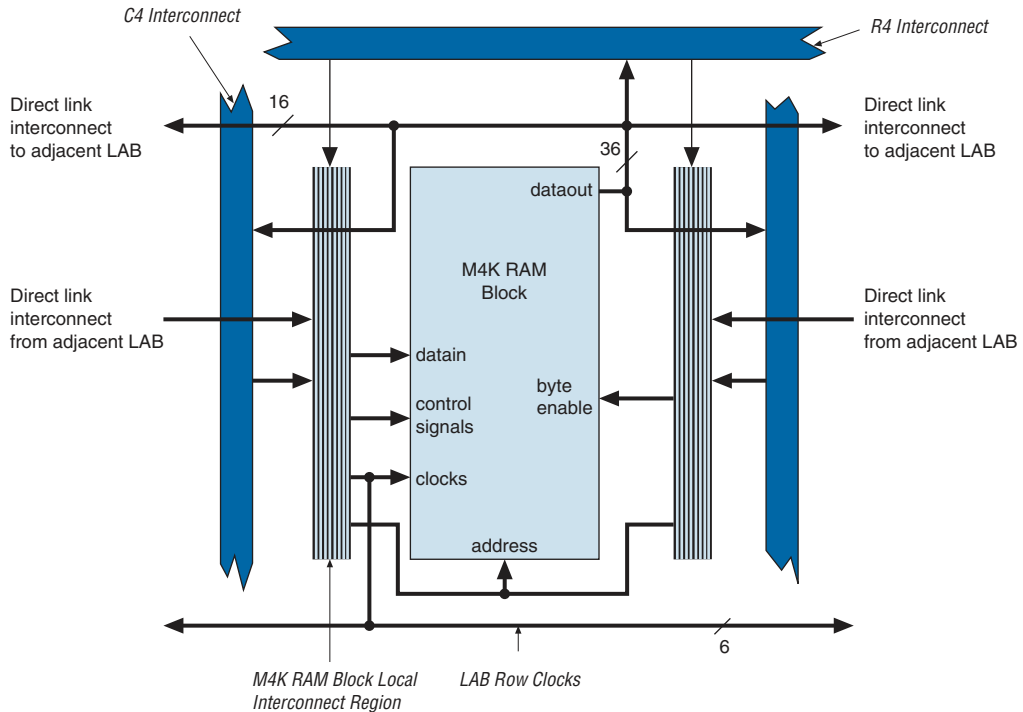
M512 RAM blocks can have different clocks on its inputs and outputs. The *wren*, *datain*, and write address registers are all clocked together from one of the two clocks feeding the block. The read address, *rden*, and output registers can be clocked by either of the two clocks driving the block, allowing the RAM block to operate in read and write or input and output clock modes. Only the output register can be bypassed. The six *labclk* signals or local interconnect can drive the *inclock*, *outclock*, *wren*, *rden*, and *outclr* signals. Because of the advanced interconnect between the LAB and M512 RAM blocks, ALMs can also control the *wren* and *rden* signals and the RAM clock, clock enable, and asynchronous clear signals. Figure 2–49 shows the M512 RAM block control signal generation logic.

Figure 2–49. M512 RAM Block Control Signals



The RAM blocks in Stratix II GX devices have local interconnects to allow ALMs and interconnects to drive into RAM blocks. The M512 RAM block local interconnect is driven by the R4, C4, and direct link interconnects from adjacent LABs. The M512 RAM blocks can communicate with LABs on either the left or right side through these row interconnects or with LAB columns on the left or right side with the column interconnects. The M512 RAM block has up to 16 direct link input connections from the left adjacent LABs and another 16 from the right adjacent LAB. M512 RAM outputs can also connect to left and right LABs through direct link interconnect. The M512 RAM block has equal opportunity for access and performance to and from LABs on either its left or right side. Figure 2–50 shows the M512 RAM block to logic array interface.

Figure 2–50. M512 RAM Block LAB Row Interface



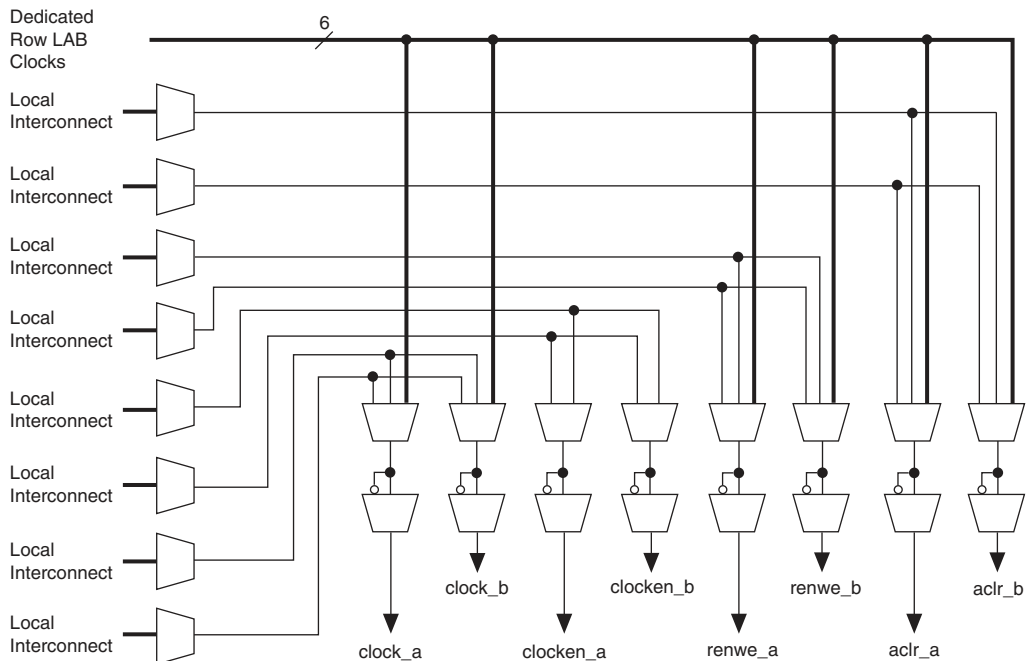
M4K RAM Blocks

The M4K RAM block includes support for true dual-port RAM. The M4K RAM block is used to implement buffers for a wide variety of applications such as storing processor code, implementing lookup schemes, and implementing larger memory applications. Each block contains 4,608 RAM bits (including parity bits). M4K RAM blocks can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

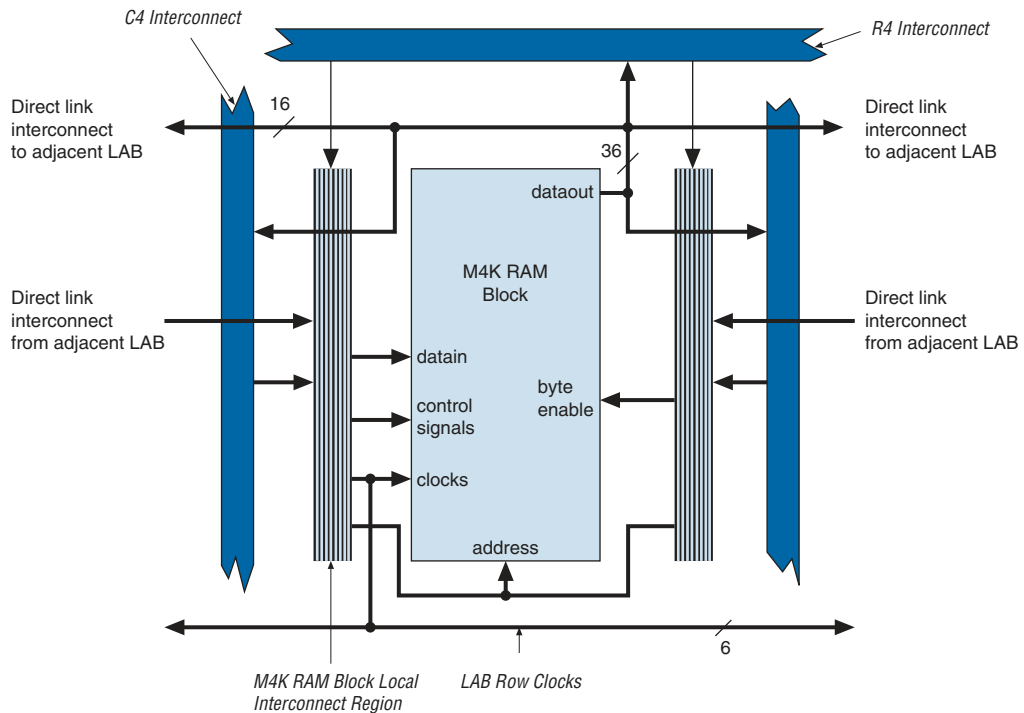
When configured as RAM or ROM, you can use an initialization file to pre-load the memory contents.

The M4K RAM blocks allow for different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M4K RAM block registers (`renwe`, `address`, `byte enable`, `datain`, and `output` registers). Only the `output` register can be bypassed. The six `labclk` signals or local interconnects can drive the control signals for the A and B ports of the M4K RAM block. ALMs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, `clr_b`, `clocken_a`, and `clocken_b` signals, as shown in [Figure 2-51](#).

Figure 2–51. M4K RAM Block Control Signals

The R4, C4, and direct link interconnects from adjacent LABs drive the M4K RAM block local interconnect. The M4K RAM blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 16 direct link input connections to the M4K RAM block are possible from the left adjacent LABs and another 16 possible from the right adjacent LAB. M4K RAM block outputs can also connect to left and right LABs through direct link interconnect. [Figure 2–52](#) shows the M4K RAM block to logic array interface.

Figure 2–52. M4K RAM Block LAB Row Interface



M-RAM Block

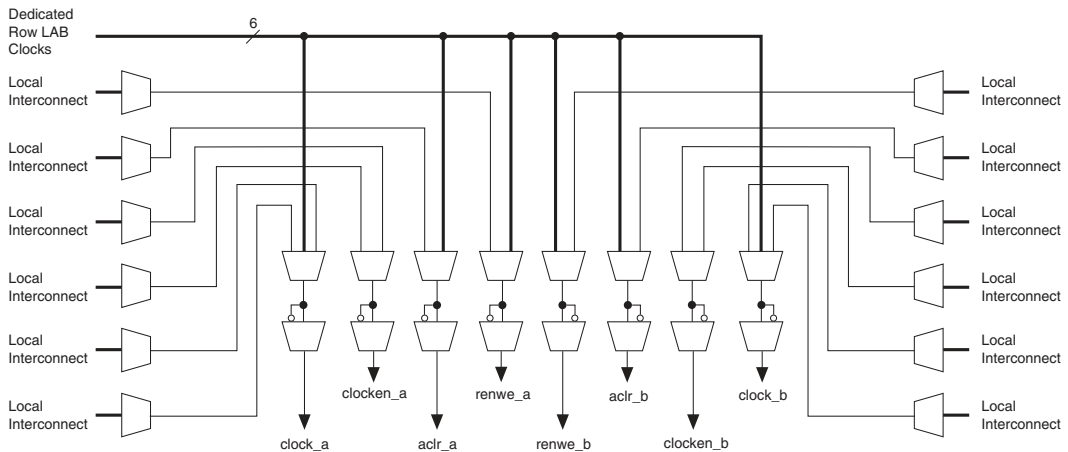
The largest TriMatrix memory block, the M-RAM block, is useful for applications where a large volume of data must be stored on-chip. Each block contains 589,824 RAM bits (including parity bits). The M-RAM block can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO

You cannot use an initialization file to initialize the contents of a M-RAM block. All M-RAM block contents power up to an undefined value. Only synchronous operation is supported in the M-RAM block, so all inputs are registered. Output registers can be bypassed.

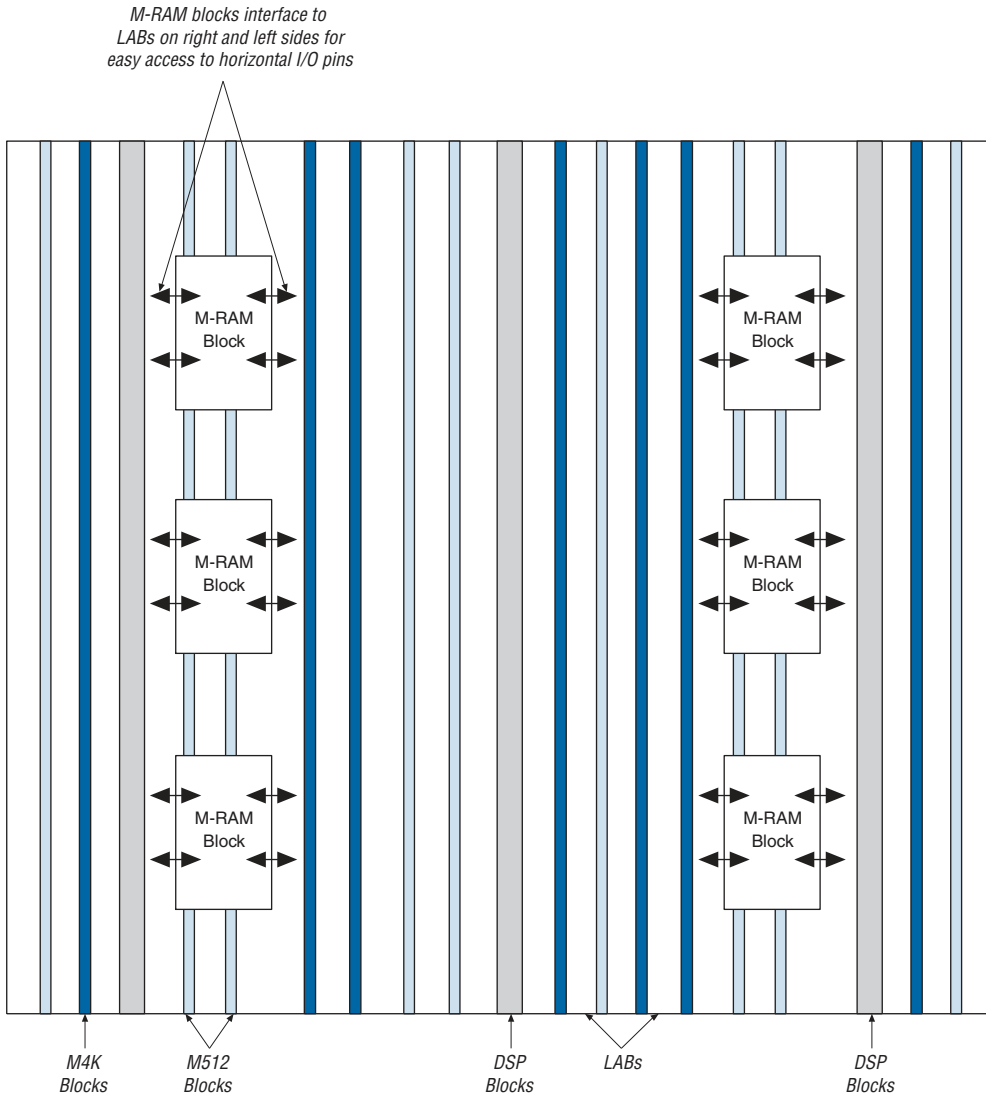
Similar to all RAM blocks, M-RAM blocks can have different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M-RAM block registers (renwe, address, byte enable, datain, and output registers). The output register can be bypassed. The six local interconnect signals or local interconnect can drive the control signals for the A and B ports of the M-RAM block. ALMs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, `clr_b`, `clocken_a`, and `clocken_b` signals, as shown in [Figure 2-53](#).

Figure 2-53. M-RAM Block Control Signals



The R4, R24, C4, and direct link interconnects from adjacent LABs on either the right or left side drive the M-RAM block local interconnect. Up to 16 direct link input connections to the M-RAM block are possible from the left adjacent LABs and another 16 possible from the right adjacent LAB. M-RAM block outputs can also connect to left and right LABs through direct link interconnect. [Figure 2-54](#) shows an example floorplan for the EP2SGX130 device and the location of the M-RAM interfaces. [Figures 2-55](#) and [2-56](#) show the interface between the M-RAM block and the logic array.

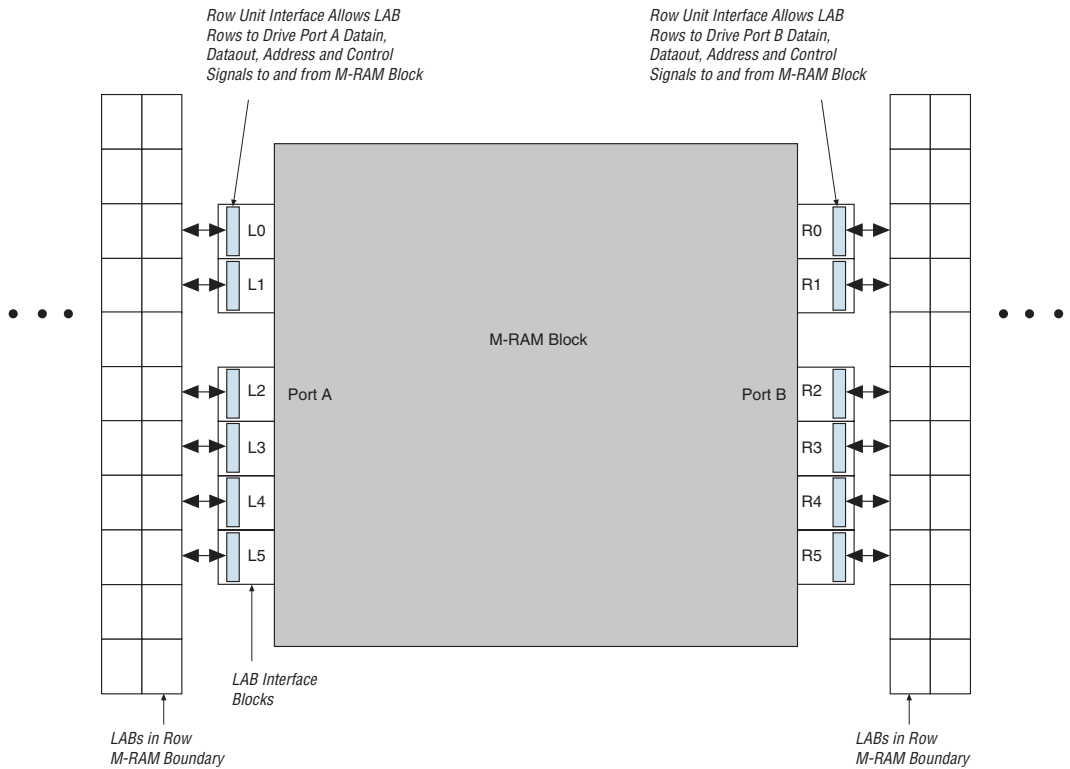
Figure 2–54. EP2SGX130 Device with M-RAM Interface Locations *Note (1)*



Note to Figure 2–54:

(1) The device shown is an EP2SGX130 device. The number and position of M-RAM blocks varies in other devices.

Figure 2-55. M-RAM Block LAB Row Interface *Note (1)*



Note to Figure 2-55:

(1) Only R24 and C16 interconnects cross the M-RAM block boundaries.

Figure 2-56. M-RAM Row Unit Interface to Interconnect

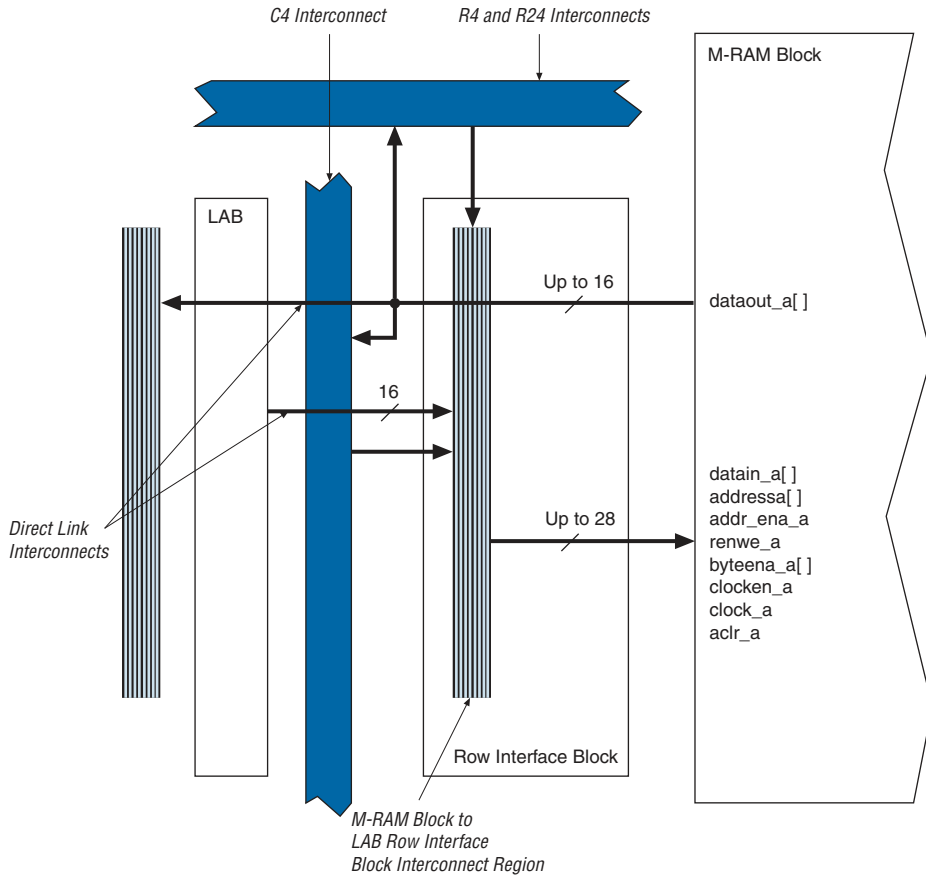


Table 2–20 shows the input and output data signal connections along with the address and control signal input connections to the row unit interfaces (L0 to L5 and R0 to R5).

| Unit Interface Block | Input Signals | Output Signals |
|-----------------------------|---|-----------------------|
| L0 | datain_a[14..0] byteena_a[1..0] | dataout_a[11..0] |
| L1 | datain_a[29..15] byteena_a[3..2] | dataout_a[23..12] |
| L2 | datain_a[35..30] addressa[4..0] addr_ena_a clock_a clocken_a renwe_a aclr_a | dataout_a[35..24] |
| L3 | addressa[15..5] datain_a[41..36] | dataout_a[47..36] |
| L4 | datain_a[56..42] byteena_a[5..4] | dataout_a[59..48] |
| L5 | datain_a[71..57] byteena_a[7..6] | dataout_a[71..60] |
| R0 | datain_b[14..0] byteena_b[1..0] | dataout_b[11..0] |
| R1 | datain_b[29..15] byteena_b[3..2] | dataout_b[23..12] |
| R2 | datain_b[35..30] addressb[4..0] addr_ena_b clock_b clocken_b renwe_b aclr_b | dataout_b[35..24] |
| R3 | addressb[15..5] datain_b[41..36] | dataout_b[47..36] |
| R4 | datain_b[56..42] byteena_b[5..4] | dataout_b[59..48] |
| R5 | datain_b[71..57] byteena_b[7..6] | dataout_b[71..60] |



Refer to the *TriMatrix Embedded Memory Blocks in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook* for more information on TriMatrix memory.

Digital Signal Processing (DSP) Block

The most commonly used DSP functions are finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, direct cosine transform (DCT) functions, and correlators. All of these use the multiplier as the fundamental building block. Additionally, some applications need specialized operations such as multiply-add and multiply-accumulate operations. Stratix II GX devices provide DSP blocks to meet the arithmetic requirements of these functions.

Each Stratix II GX device has two to four columns of DSP blocks to efficiently implement DSP functions faster than ALM-based implementations. Stratix II GX devices have up to 24 DSP blocks per column (see [Table 2–21](#)). Each DSP block can be configured to support up to:

- Eight 9×9 -bit multipliers
- Four 18×18 -bit multipliers
- One 36×36 -bit multiplier

As indicated, the Stratix II GX DSP block can support one 36×36 -bit multiplier in a single DSP block, and is true for any combination of signed, unsigned, or mixed sign multiplications.

Figures 2–57 shows one of the columns with surrounding LAB rows.

Figure 2–57. DSP Blocks Arranged in Columns

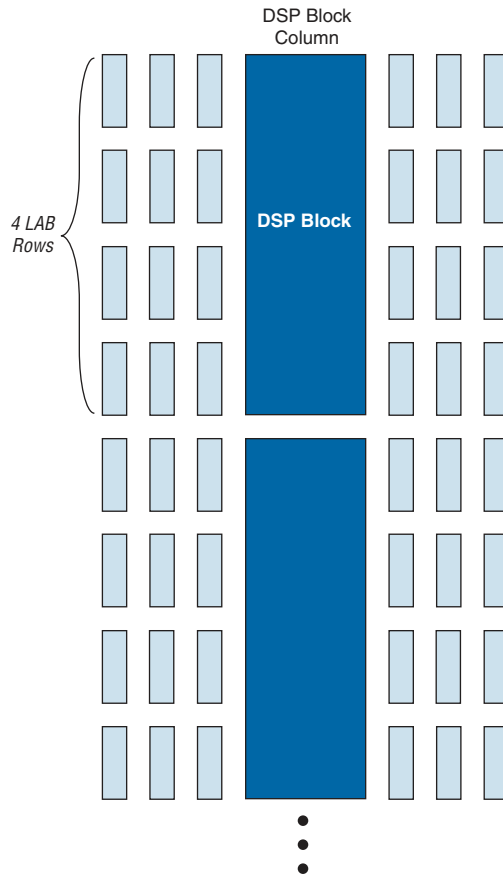


Table 2–21 shows the number of DSP blocks in each Stratix II GX device. DSP block multipliers can optionally feed an adder/subtractor or accumulator in the block, depending on the configuration, which makes routing to ALMs easier, saves ALM routing resources, and increases performance because all connections and blocks are in the DSP block.

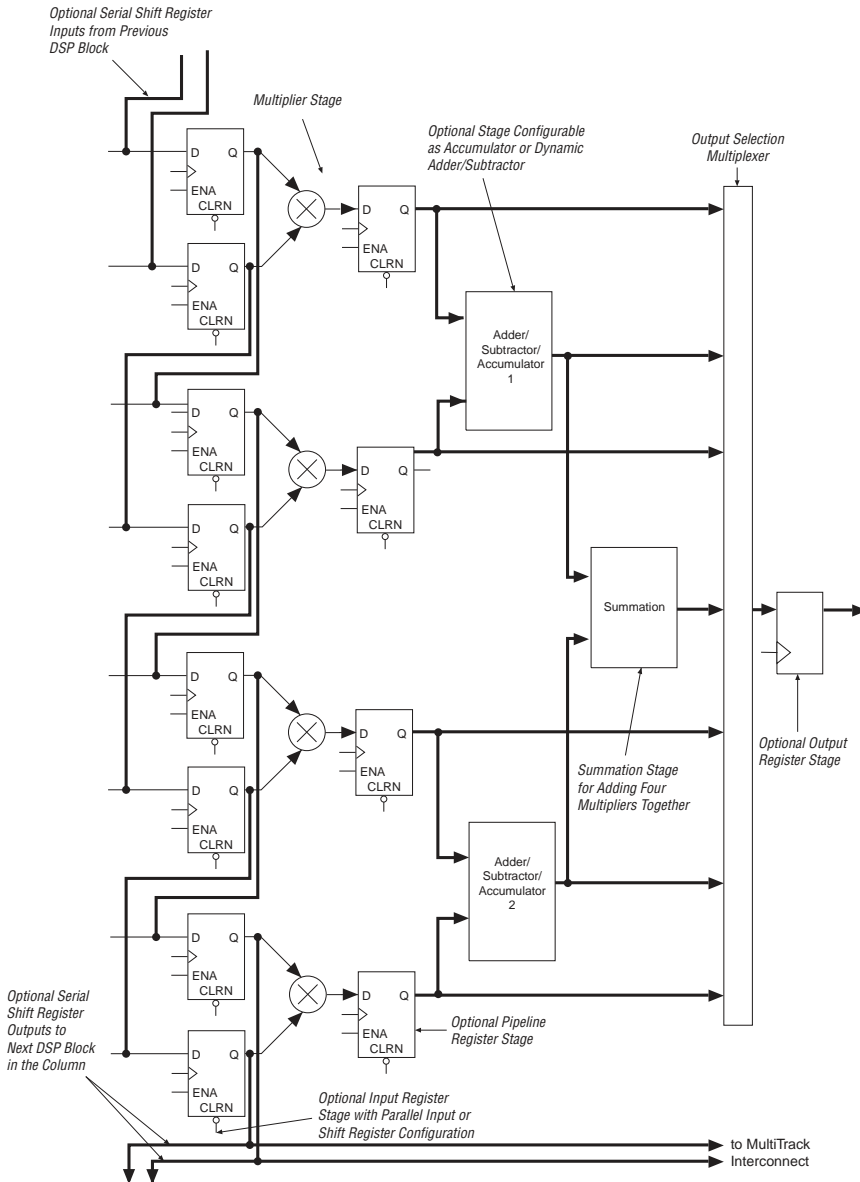
| Device | DSP Blocks | Total 9 × 9 Multipliers | Total 18 × 18 Multipliers | Total 36 × 36 Multipliers |
|-----------|------------|-------------------------|---------------------------|---------------------------|
| EP2SGX30 | 16 | 128 | 64 | 16 |
| EP2SGX60 | 36 | 288 | 144 | 36 |
| EP2SGX90 | 48 | 384 | 192 | 48 |
| EP2SGX130 | 63 | 504 | 252 | 63 |

Note to Table 2–21:

- (1) This list only shows functions that can fit into a single DSP block. Multiple DSP blocks can support larger multiplication functions.

Additionally, the DSP block input registers can efficiently implement shift registers for FIR filter applications, and DSP blocks support Q1.15 format rounding and saturation. Figure 2–58 shows the top-level diagram of the DSP block configured for 18 × 18-bit multiplier mode.

Figure 2–58. DSP Block Diagram for 18 × 18-Bit Configuration



Modes of Operation

The adder, subtractor, and accumulate functions of a DSP block have four modes of operation:

- Simple multiplier
- Multiply-accumulator
- Two-multipliers adder
- Four-multipliers adder

Table 2–22 shows the different number of multipliers possible in each DSP block mode according to size. These modes allow the DSP blocks to implement numerous applications for DSP including FFTs, complex FIR, FIR, 2D FIR filters, equalizers, IIR, correlators, matrix multiplication, and many other functions. The DSP blocks also support mixed modes and mixed multiplier sizes in the same block. For example, half of one DSP block can implement one 18×18 -bit multiplier in multiply-accumulator mode, while the other half of the DSP block implements four 9×9 -bit multipliers in simple multiplier mode.

| DSP Block Mode | 9×9 | 18×18 | 36×36 |
|------------------------|---|--|--|
| Multiplier | Eight multipliers with eight product outputs | Four multipliers with four product outputs | One multiplier with one product output |
| Multiply-accumulator | — | Two 52-bit multiply-accumulate blocks | — |
| Two-multipliers adder | Four two-multiplier adder (two 9×9 complex multiply) | Two two-multiplier adder (one 18×18 complex multiply) | — |
| Four-multipliers adder | Two four-multiplier adder | One four-multiplier adder | — |

DSP Block Interface

The Stratix II GX device DSP block input registers can generate a shift register that can cascade down in the same DSP block column. Dedicated connections between DSP blocks provide fast connections between the shift register inputs to cascade the shift register chains. You can cascade registers within multiple DSP blocks for 9×9 - or 18×18 -bit FIR filters larger than four taps, with additional adder stages implemented in ALMs. If the DSP block is configured as 36×36 bits, the adder, subtractor, or accumulator stages are implemented in ALMs. Each DSP block can route the shift register chain out of the block to cascade multiple columns of DSP blocks.

The DSP block is divided into four block units that interface with four LAB rows on the left and right. Each block unit can be considered one complete 18×18 -bit multiplier with 36 inputs and 36 outputs. A local interconnect region is associated with each DSP block. Like a LAB, this interconnect region can be fed with 16 direct link interconnects from the LAB to the left or right of the DSP block in the same row. R4 and C4 routing resources can access the DSP block's local interconnect region. The outputs also work similarly to LAB outputs. Eighteen outputs from the DSP block can drive to the left LAB through direct link interconnects and 18 can drive to the right LAB through direct link interconnects. All 36 outputs can drive to R4 and C4 routing interconnects. Outputs can drive right- or left-column routing.

Figures 2–59 and 2–60 show the DSP block interfaces to LAB rows.

Figure 2–59. DSP Block Interconnect Interface

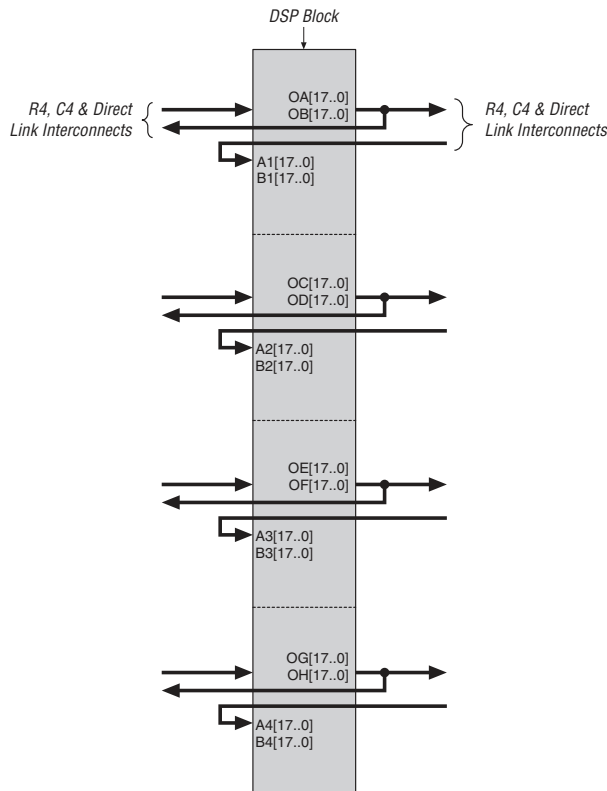
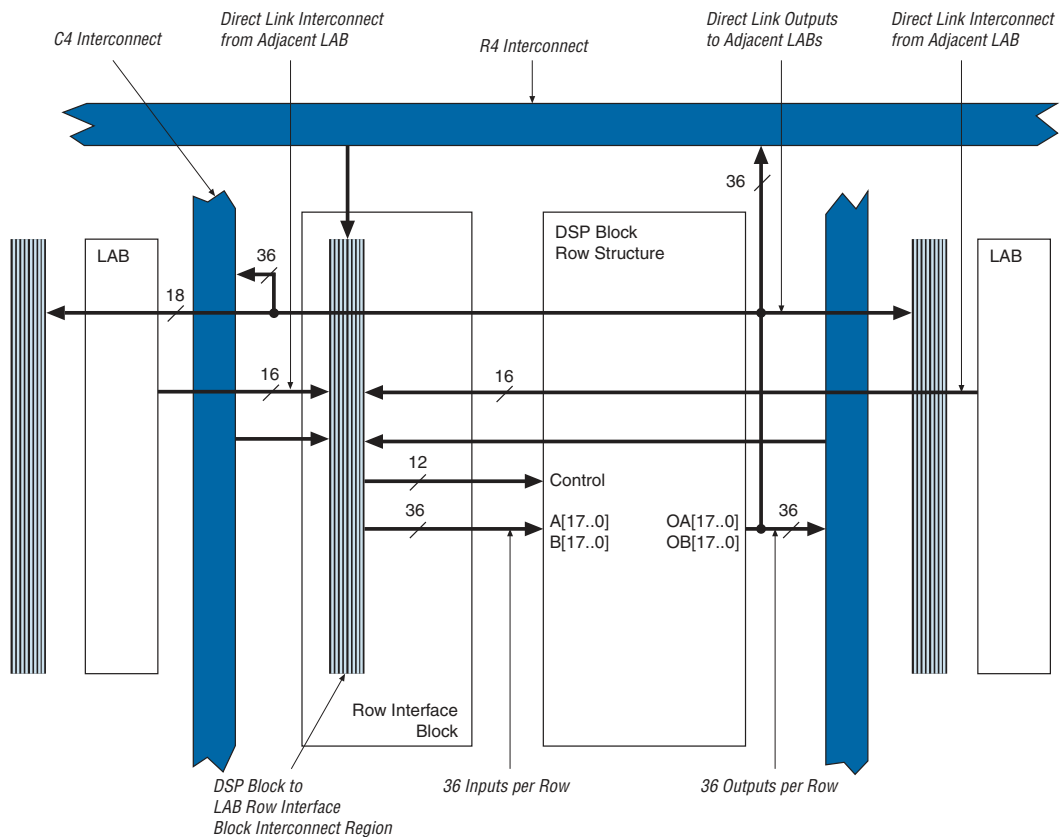


Figure 2–60. DSP Block Interface to Interconnect



A bus of 44 control signals feeds the entire DSP block. These signals include clocks, asynchronous clears, clock enables, signed and unsigned control signals, addition and subtraction control signals, rounding and saturation control signals, and accumulator synchronous loads. The clock signals are routed from LAB row clocks and are generated from specific LAB rows at the DSP block interface. The LAB row source for control signals, data inputs, and outputs is shown in [Table 2–23](#).



Refer to the *DSP Blocks in Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook* for more information on DSP blocks.

Table 2–23. DSP Block Signal Sources and Destinations

| LAB Row at Interface | Control Signals Generated | Data Inputs | Data Outputs |
|----------------------|--|--------------------------|--------------------------|
| 0 | clock0 aclr0 ena0 mult01_saturate addnsub1_round/ accum_round addnsub1 signa sourcea sourceb | A1 [17..0] B1 [17..0] | OA [17..0] OB [17..0] |
| 1 | clock1 aclr1 ena1 accum_saturate mult01_round accum_sload sourcea sourceb mode0 | A2 [17..0] B2 [17..0] | OC [17..0] OD [17..0] |
| 2 | clock2 aclr2 ena2 mult23_saturate addnsub3_round/ accum_round addnsub3 sign_b sourcea sourceb | A3 [17..0] B3 [17..0] | OE [17..0] OF [17..0] |
| 3 | clock3 aclr3 ena3 accum_saturate mult23_round accum_sload sourcea sourceb mode1 | A4 [17..0] B4 [17..0] | OG [17..0] OH [17..0] |

PLLs and Clock Networks

Stratix II GX devices provide a hierarchical clock structure and multiple phase-locked loops (PLLs) with advanced features. The large number of clocking resources in combination with the clock synthesis precision provided by enhanced and fast PLLs provides a complete clock management solution.

Global and Hierarchical Clocking

Stratix II GX devices provide 16 dedicated global clock networks and 32 regional clock networks (eight per device quadrant). These clocks are organized into a hierarchical clock structure that allows for up to 24 clocks per device region with low skew and delay. This hierarchical clocking scheme provides up to 48 unique clock domains in Stratix II GX devices.

There are 12 dedicated clock pins to drive either the global or regional clock networks. Four clock pins drive each side of the device, as shown in [Figures 2–61](#) and [2–62](#). Internal logic and enhanced and fast PLL outputs can also drive the global and regional clock networks. Each global and regional clock has a clock control block, which controls the selection of the clock source and dynamically enables or disables the clock to reduce power consumption. [Table 2–24](#) shows global and regional clock features.

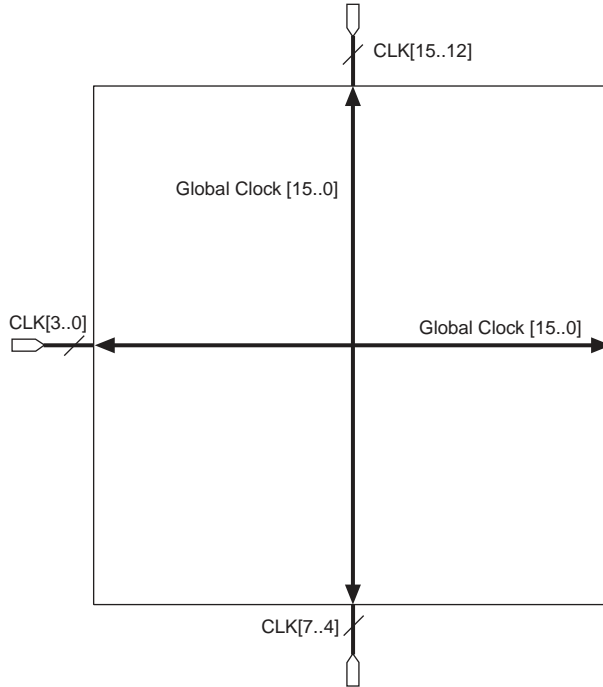
| <i>Table 2–24. Global and Regional Clock Features</i> | | |
|---|--|--|
| Feature | Global Clocks | Regional Clocks |
| Number per device | 16 | 32 |
| Number available per quadrant | 16 | 8 |
| Sources | Clock pins, PLL outputs, core routings, inter-transceiver clocks | Clock pins, PLL outputs, core routings, inter-transceiver clocks |
| Dynamic clock source selection | ✓ | — |
| Dynamic enable/disable | ✓ | ✓ |

Global Clock Network

These clocks drive throughout the entire device, feeding all device quadrants. The global clock networks can be used as clock sources for all resources in the device IOEs, ALMs, DSP blocks, and all memory blocks. These resources can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin. The global clock networks can also be driven by internal logic for internally

generated global clocks and asynchronous clears, clock enables, or other control signals with large fanout. Figure 2–61 shows the 12 dedicated CLK pins driving global clock networks.

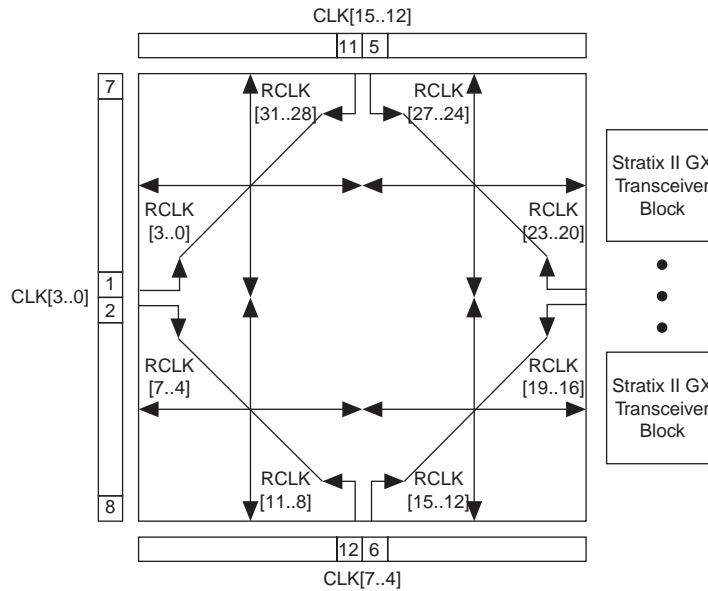
Figure 2–61. Global Clocking



Regional Clock Network

There are eight regional clock networks (RCLK [7 . . 0]) in each quadrant of the Stratix II GX device that are driven by the dedicated CLK [15 . . 12] and CLK [7 . . 0] input pins, by PLL outputs, or by internal logic. The regional clock networks provide the lowest clock delay and skew for logic contained in a single quadrant. The CLK pins symmetrically drive the RCLK networks in a particular quadrant, as shown in Figure 2–62.

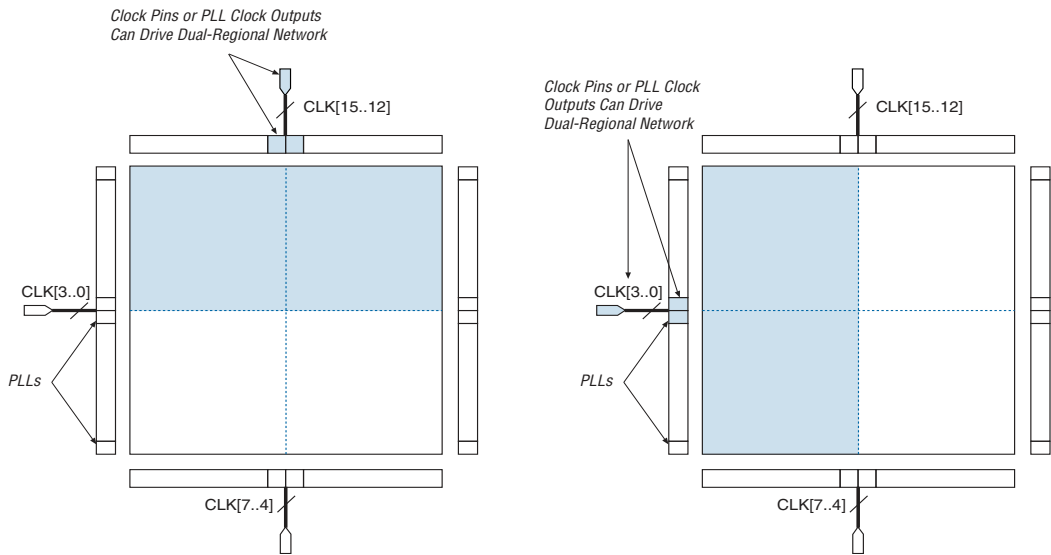
Figure 2–62. Regional Clocks



Dual-Regional Clock Network

A single source (CLK pin or PLL output) can generate a dual-regional clock by driving two regional clock network lines in adjacent quadrants (one from each quadrant), which allows logic that spans multiple quadrants to utilize the same low skew clock. The routing of this clock signal on an entire side has approximately the same speed but slightly higher clock skew when compared with a clock signal that drives a single quadrant. Internal logic-array routing can also drive a dual-regional clock. Clock pins and enhanced PLL outputs on the top and bottom can drive horizontal dual-regional clocks. Clock pins and fast PLL outputs on the left and right can drive vertical dual-regional clocks, as shown in [Figure 2–63](#). Corner PLLs cannot drive dual-regional clocks.

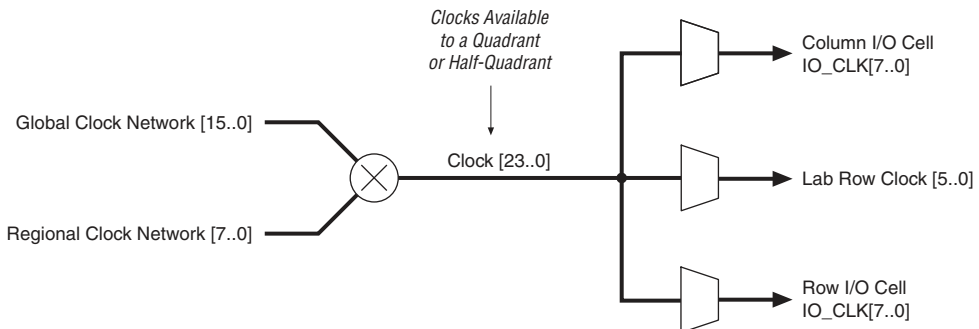
Figure 2–63. Dual-Regional Clocks



Combined Resources

Within each quadrant, there are 24 distinct dedicated clocking resources consisting of 16 global clock lines and 8 regional clock lines. Multiplexers are used with these clocks to form buses to drive LAB row clocks, column IOE clocks, or row IOE clocks. Another multiplexer is used at the LAB level to select three of the six row clocks to feed the ALM registers in the LAB (see [Figure 2–64](#)).

Figure 2–64. Hierarchical Clock Networks per Quadrant



IOE clocks have row and column block regions that are clocked by 8 I/O clock signals chosen from the 24 quadrant clock resources. Figures 2-65 and 2-66 show the quadrant relationship to the I/O clock regions.

Figure 2-65. EP2SGX30 Device I/O Clock Groups

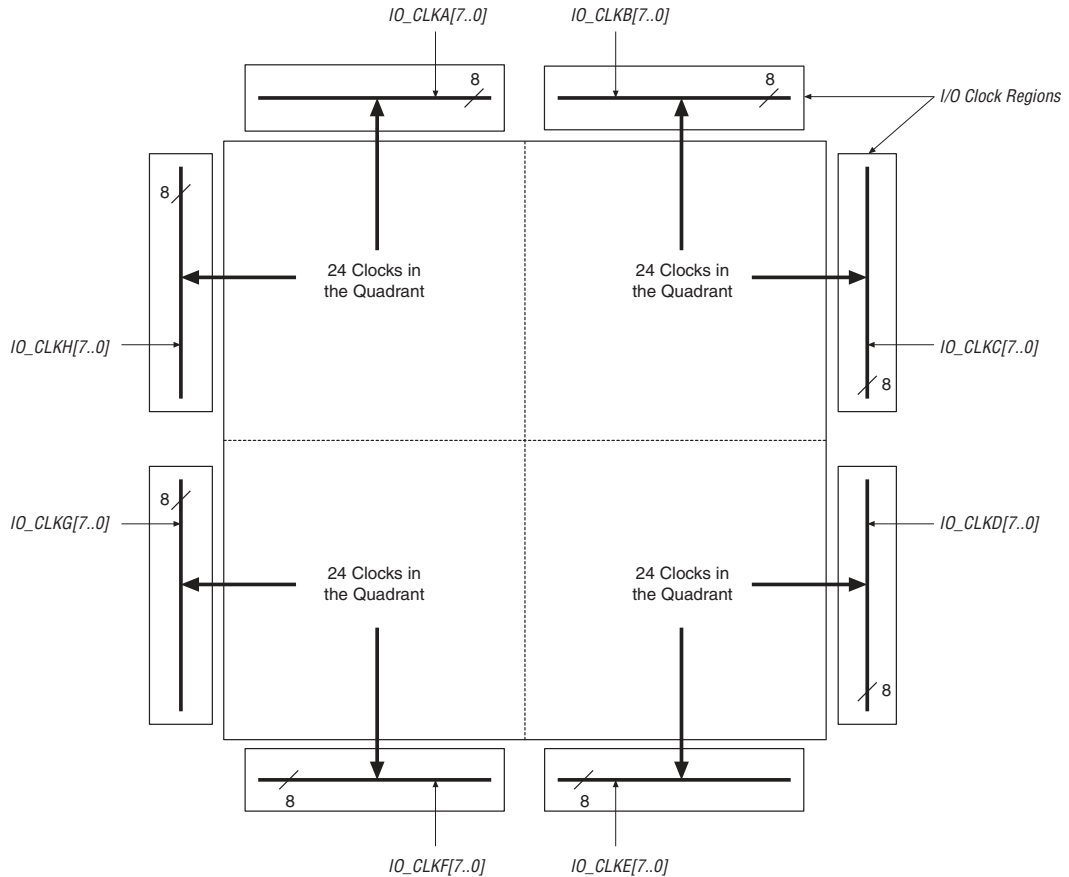
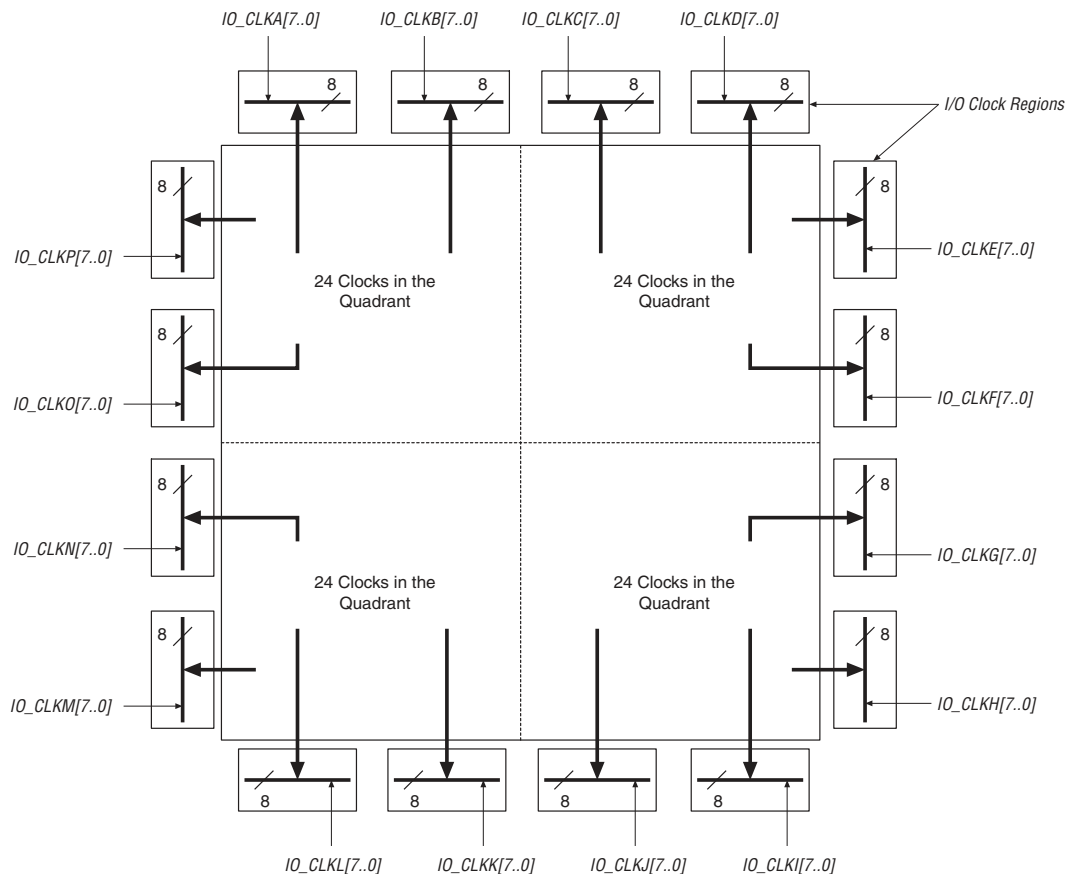


Figure 2–66. EP2SGX60, EP2SGX90 and EP2SGX130 Device I/O Clock Groups



You can use the Quartus II software to control whether a clock input pin drives either a global, regional, or dual-regional clock network. The Quartus II software automatically selects the clocking resources if not specified.

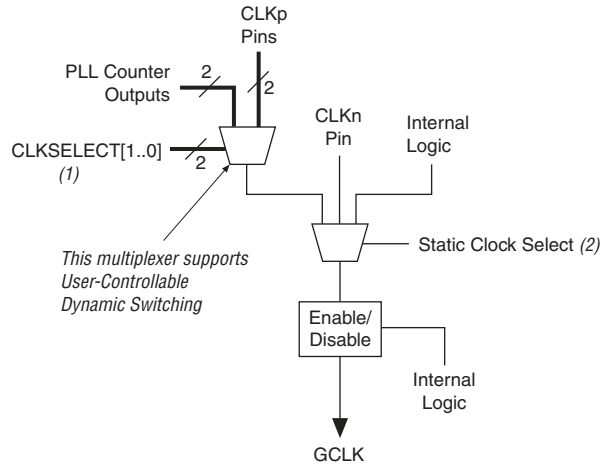
Clock Control Block

Each global clock, regional clock, and PLL external clock output has its own clock control block. The control block has two functions:

- Clock source selection (dynamic selection for global clocks)
- Clock power-down (dynamic clock enable or disable)

Figures 2–67 through 2–69 show the clock control block for the global clock, regional clock, and PLL external clock output, respectively.

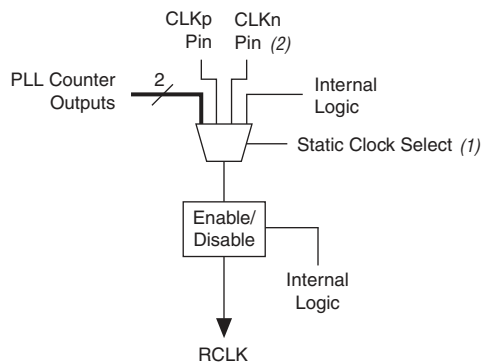
Figure 2–67. Global Clock Control Blocks



Notes to Figure 2–67:

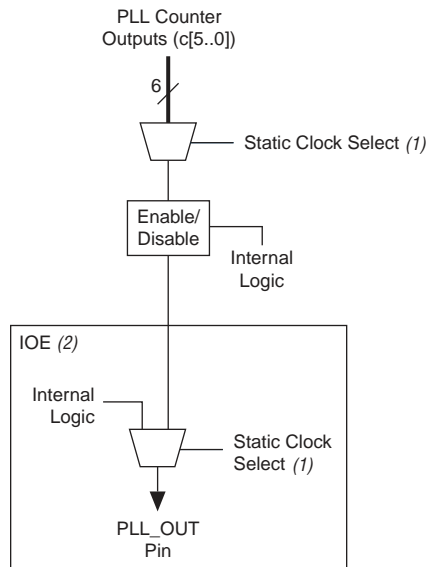
- (1) These clock select signals can be dynamically controlled through internal logic when the device is operating in user mode.
- (2) These clock select signals can only be set through a configuration file (SRAM Object File [.sof] or Programmer Object File [.pof]) and cannot be dynamically controlled during user mode operation.

Figure 2–68. Regional Clock Control Blocks



Notes to Figure 2–68:

- (1) These clock select signals can only be set through a configuration file (.sof or .pof) and cannot be dynamically controlled during user mode operation.
- (2) Only the CLKn pins on the top and bottom of the device feed to regional clock select.

Figure 2–69. External PLL Output Clock Control Blocks**Notes to Figure 2–69:**

- (1) These clock select signals can only be set through a configuration file (.sof or .pof) and cannot be dynamically controlled during user mode operation.
- (2) The clock control block feeds to a multiplexer within the PLL_OUT pin's IOE. The PLL_OUT pin is a dual-purpose pin. Therefore, this multiplexer selects either an internal signal or the output of the clock control block.

For the global clock control block, the clock source selection can be controlled either statically or dynamically. You have the option of statically selecting the clock source by using the Quartus II software to set specific configuration bits in the configuration file (.sof or .pof) or you can control the selection dynamically by using internal logic to drive the multiplexer select inputs. When selecting statically, the clock source can be set to any of the inputs to the select multiplexer. When selecting the clock source dynamically, you can either select between two PLL outputs (such as the C0 or C1 outputs from one PLL), between two PLLs (such as the C0/C1 clock output of one PLL or the C0/C1 clock output of the other PLL), between two clock pins (such as CLK0 or CLK1), or between a combination of clock pins or PLL outputs.

For the regional and PLL_OUT clock control block, the clock source selection can only be controlled statically using configuration bits. Any of the inputs to the clock select multiplexer can be set as the clock source.

The Stratix II GX clock networks can be disabled (powered down) by both static and dynamic approaches. When a clock net is powered down, all the logic fed by the clock net is in an off-state, thereby reducing the overall power consumption of the device. The global and regional clock networks can be powered down statically through a setting in the configuration file (.sof or .pof). Clock networks that are not used are automatically powered down through configuration bit settings in the configuration file generated by the Quartus II software. The dynamic clock enable and disable feature allows the internal logic to control power up and down synchronously on GCLK and RCLK nets and PLL_OUT pins. This function is independent of the PLL and is applied directly on the clock network or PLL_OUT pin, as shown in [Figures 2-67 through 2-69](#).

Enhanced and Fast PLLs

Stratix II GX devices provide robust clock management and synthesis using up to four enhanced PLLs and four fast PLLs. These PLLs increase performance and provide advanced clock interfacing and clock frequency synthesis. With features such as clock switchover, spread spectrum clocking, reconfigurable bandwidth, phase control, and reconfigurable phase shifting, the Stratix II GX device's enhanced PLLs provide you with complete control of clocks and system timing. The fast PLLs provide general purpose clocking with multiplication and phase shifting as well as high-speed outputs for high-speed differential I/O support. Enhanced and fast PLLs work together with the Stratix II GX high-speed I/O and advanced clock architecture to provide significant improvements in system performance and bandwidth.

The Quartus II software enables the PLLs and their features without requiring any external devices. Table 2–25 shows the PLLs available for each Stratix II GX device and their type.

Table 2–25. Stratix II GX Device PLL Availability *Notes (1), (2)*

| Device | Fast PLLs | | | | | | | | Enhanced PLLs | | | |
|-----------|-----------|---|-------|-------|---|---|-------|--------|---------------|---|----|----|
| | 1 | 2 | 3 (3) | 4 (3) | 7 | 8 | 9 (3) | 10 (3) | 5 | 6 | 11 | 12 |
| EP2SGX30 | ✓ | ✓ | | | | | | | ✓ | ✓ | | |
| EP2SGX60 | ✓ | ✓ | | | ✓ | ✓ | | | ✓ | ✓ | ✓ | ✓ |
| EP2SGX90 | ✓ | ✓ | | | ✓ | ✓ | | | ✓ | ✓ | ✓ | ✓ |
| EP2SGX130 | ✓ | ✓ | | | ✓ | ✓ | | | ✓ | ✓ | ✓ | ✓ |

Notes to Table 2–25:

- (1) EP2SGX30C/D and EP2SGX60C/D devices only have two fast PLLs (1 and 2), but the connectivity from these two PLLs to the global and regional clock networks remains the same as shown. The EP2S60C/D devices only have two enhanced PLLs (5 and 6).
- (2) The global or regional clocks in a fast PLL’s quadrant can drive the fast PLL input. A dedicated clock input pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.
- (3) PLLs 3, 4, 9, and 10 are not available in Stratix II GX devices. However, these PLLs are listed in Table 2–25 because the Stratix II GX PLL numbering scheme is consistent with Stratix and Stratix II devices.

Table 2–26 shows the enhanced PLL and fast PLL features in Stratix II GX devices.

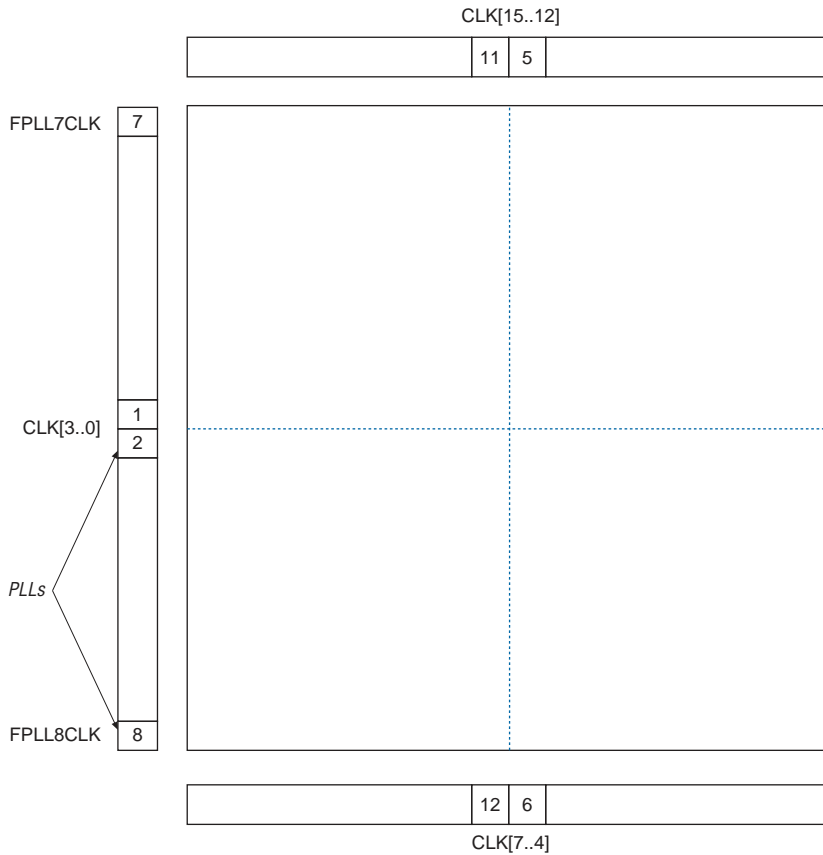
| Feature | Enhanced PLL | Fast PLL |
|-----------------------------------|--|--|
| Clock multiplication and division | $m/(n \times \text{post-scale counter})$ (1) | $m/(n \times \text{post-scale counter})$ (2) |
| Phase shift | Down to 125-ps increments (3), (4) | Down to 125-ps increments (3), (4) |
| Clock switchover | ✓ | ✓ (5) |
| PLL reconfiguration | ✓ | ✓ |
| Reconfigurable bandwidth | ✓ | ✓ |
| Spread spectrum clocking | ✓ | |
| Programmable duty cycle | ✓ | ✓ |
| Number of internal clock outputs | 6 | 4 |
| Number of external clock outputs | Three differential/six single-ended | (6) |
| Number of feedback clock inputs | One single-ended or differential (7), (8) | |

Notes to Table 2–26:

- (1) For enhanced PLLs, m , n range from 1 to 256 and post-scale counters range from 1 to 512 with 50% duty cycle.
- (2) For fast PLLs, m , and post-scale counters range from 1 to 32. The n counter ranges from 1 to 4.
- (3) The smallest phase shift is determined by the voltage controlled oscillator (VCO) period divided by 8.
- (4) For degree increments, Stratix II GX devices can shift all output frequencies in increments of at least 45. Smaller degree increments are possible depending on the frequency and divide parameters.
- (5) Stratix II GX fast PLLs only support manual clock switchover.
- (6) Fast PLLs can drive to any I/O pin as an external clock. For high-speed differential I/O pins, the device uses a data channel to generate `txclkout`.
- (7) If the feedback input is used, you will lose one (or two, if f_{BIN} is differential) external clock output pin.
- (8) Every Stratix II GX device has at least two enhanced PLLs with one single-ended or differential external feedback input per PLL.

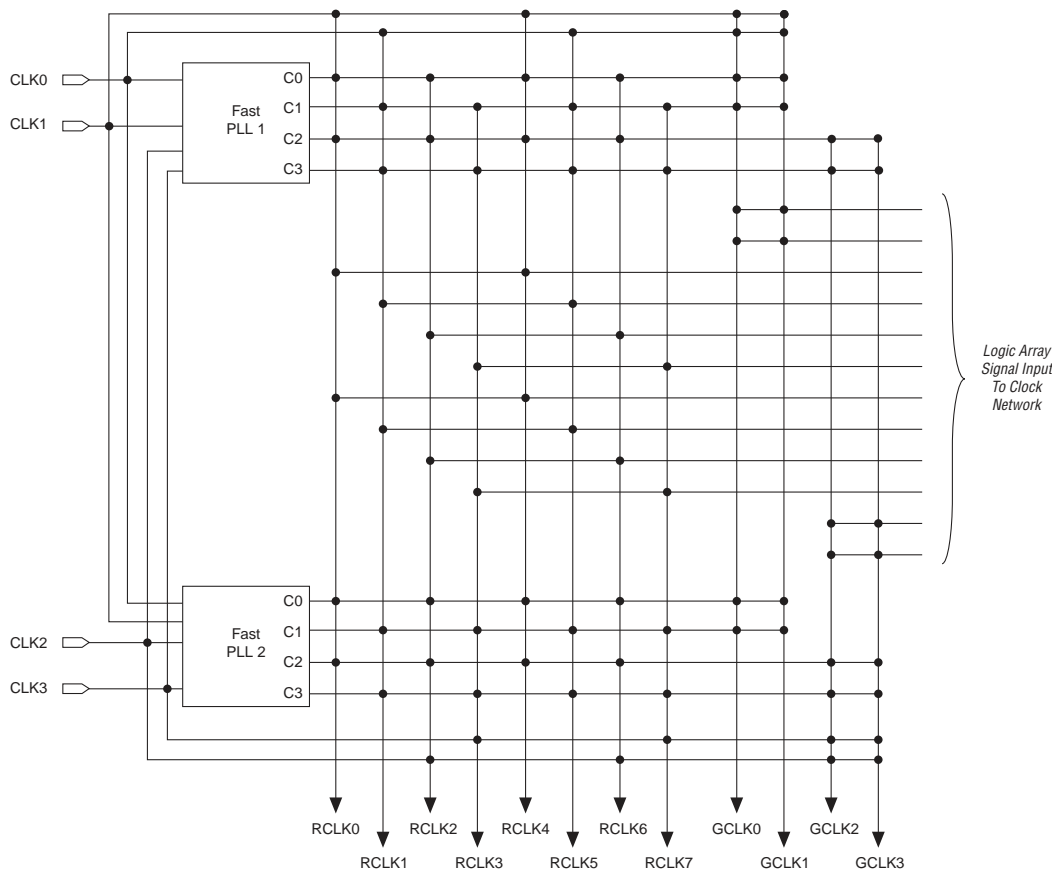
Figure 2–70 shows a top-level diagram of the Stratix II GX device and PLL floorplan.

Figure 2–70. PLL Locations



Figures 2–71 and 2–72 shows global and regional clocking from the fast PLL outputs and the side clock pins. The connections to the global and regional clocks from the fast PLL outputs, internal drivers, and the CLK pins on the left side of the device are shown in Table 2–27.

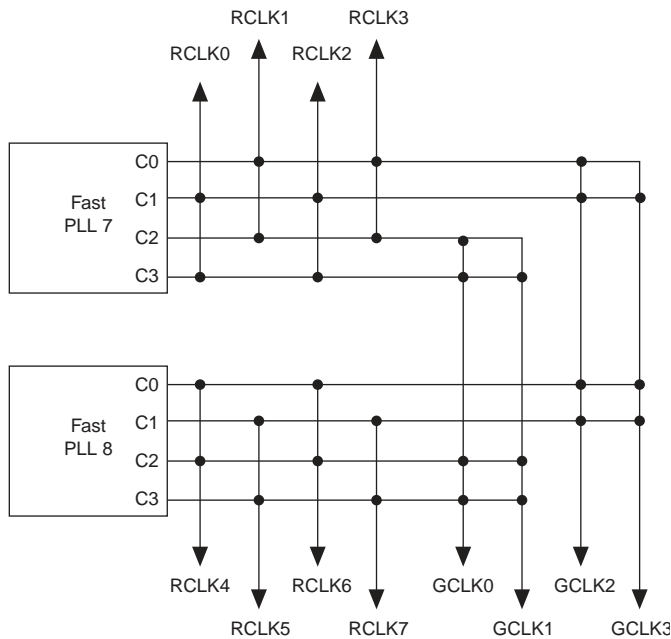
Figure 2-71. Global and Regional Clock Connections from Center Clock Pins and Fast PLL Outputs *Notes (1), (2)*



Notes to Figure 2-71:

- (1) EP2SGX30C/D and P2SGX60C/D devices only have two fast PLLs (1 and 2) and two Enhanced PLLs (5 and 6), but the connectivity from these PLLs to the global and regional clock networks remains the same as shown.
- (2) The global or regional clocks in a fast PLL's quadrant can drive the fast PLL input. A dedicated clock input pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

Figure 2–72. Global and Regional Clock Connections from Corner Clock Pins and Fast PLL Outputs *Notes (1), (2)*



Notes to Figure 2–72:

- (1) The global or regional clocks in a fast PLL’s quadrant can drive the fast PLL input. A dedicated clock input pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.
- (2) EP2SGX30C/D and EP2SGX60C/D devices only have two fast PLLs (1 and 2); they do not contain corner fast PLLs.

Table 2–27. Global and Regional Clock Connections from Left Side Clock Pins and Fast PLL Outputs (Part 1 of 3)

| Left Side Global and Regional Clock Network Connectivity | CLK0 | CLK1 | CLK2 | CLK3 | RCLK0 | RCLK1 | RCLK2 | RCLK3 | RCLK4 | RCLK5 | RCLK6 | RCLK7 |
|--|------|------|------|------|-------|-------|-------|-------|-------|-------|-------|-------|
| Clock pins | | | | | | | | | | | | |
| CLK0p | ✓ | ✓ | | | ✓ | | | | ✓ | | | |
| CLK1p | ✓ | ✓ | | | | ✓ | | | | ✓ | | |
| CLK2p | | | ✓ | ✓ | | | ✓ | | | | ✓ | |
| CLK3p | | | ✓ | ✓ | | | | ✓ | | | | ✓ |

**Table 2–27. Global and Regional Clock Connections from Left Side Clock Pins and Fast PLL Outputs
(Part 2 of 3)**

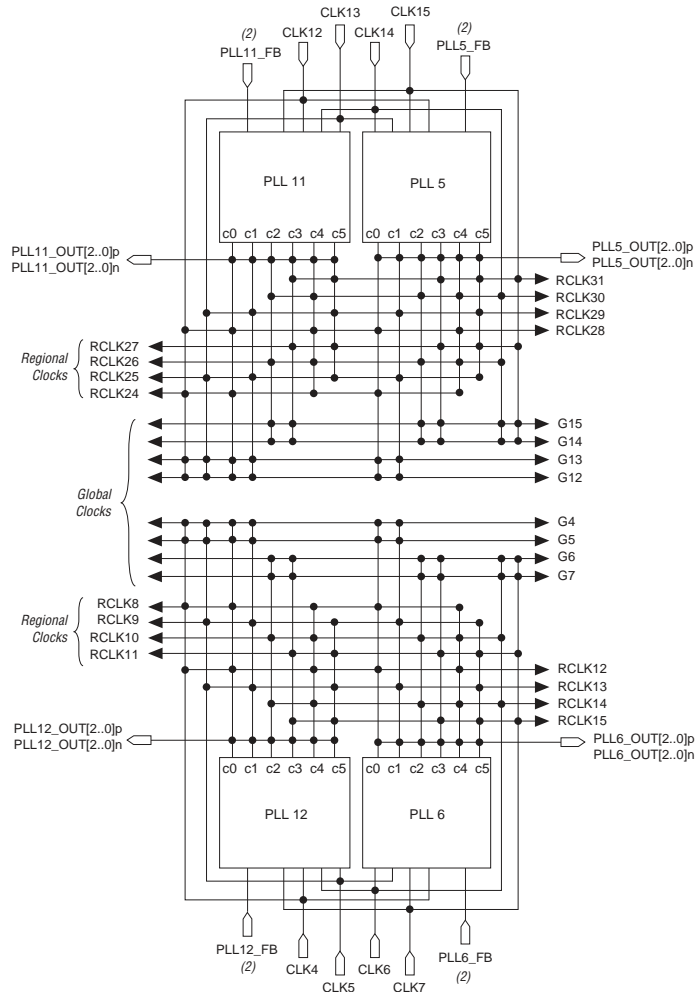
| Left Side Global and Regional Clock Network Connectivity | CLK0 | CLK1 | CLK2 | CLK3 | RCLK0 | RCLK1 | RCLK2 | RCLK3 | RCLK4 | RCLK5 | RCLK6 | RCLK7 |
|--|------|------|------|------|-------|-------|-------|-------|-------|-------|-------|-------|
| Drivers from internal logic | | | | | | | | | | | | |
| GCLKDRV0 | ✓ | ✓ | | | | | | | | | | |
| GCLKDRV1 | ✓ | ✓ | | | | | | | | | | |
| GCLKDRV2 | | | ✓ | ✓ | | | | | | | | |
| GCLKDRV3 | | | ✓ | ✓ | | | | | | | | |
| RCLKDRV0 | | | | | ✓ | | | | ✓ | | | |
| RCLKDRV1 | | | | | | ✓ | | | | ✓ | | |
| RCLKDRV2 | | | | | | | ✓ | | | | ✓ | |
| RCLKDRV3 | | | | | | | | ✓ | | | | ✓ |
| RCLKDRV4 | | | | | ✓ | | | | ✓ | | | |
| RCLKDRV5 | | | | | | ✓ | | | | ✓ | | |
| RCLKDRV6 | | | | | | | ✓ | | | | ✓ | |
| RCLKDRV7 | | | | | | | | ✓ | | | | ✓ |
| PLL 1 outputs | | | | | | | | | | | | |
| c0 | ✓ | ✓ | | | ✓ | | ✓ | | ✓ | | ✓ | |
| c1 | ✓ | ✓ | | | | ✓ | | ✓ | | ✓ | | ✓ |
| c2 | | | ✓ | ✓ | ✓ | | ✓ | | ✓ | | ✓ | |
| c3 | | | ✓ | ✓ | | ✓ | | ✓ | | ✓ | | ✓ |
| PLL 2 outputs | | | | | | | | | | | | |
| c0 | ✓ | ✓ | | | | ✓ | | ✓ | | ✓ | | ✓ |
| c1 | ✓ | ✓ | | | ✓ | | ✓ | | ✓ | | ✓ | |
| c2 | | | ✓ | ✓ | | ✓ | | ✓ | | ✓ | | ✓ |
| c3 | | | ✓ | ✓ | ✓ | | ✓ | | ✓ | | ✓ | |
| PLL 7 outputs | | | | | | | | | | | | |
| c0 | | | ✓ | ✓ | | ✓ | | ✓ | | | | |
| c1 | | | ✓ | ✓ | ✓ | | ✓ | | | | | |
| c2 | ✓ | ✓ | | | | ✓ | | ✓ | | | | |
| c3 | ✓ | ✓ | | | ✓ | | ✓ | | | | | |

**Table 2–27. Global and Regional Clock Connections from Left Side Clock Pins and Fast PLL Outputs
(Part 3 of 3)**

| Left Side Global and Regional Clock Network Connectivity | CLK0 | CLK1 | CLK2 | CLK3 | RCLK0 | RCLK1 | RCLK2 | RCLK3 | RCLK4 | RCLK5 | RCLK6 | RCLK7 |
|--|------|------|------|------|-------|-------|-------|-------|-------|-------|-------|-------|
| PLL 8 outputs | | | | | | | | | | | | |
| c0 | | | ✓ | ✓ | | | | | ✓ | | ✓ | |
| c1 | | | ✓ | ✓ | | | | | | ✓ | | ✓ |
| c2 | ✓ | ✓ | | | | | | | ✓ | | ✓ | |
| c3 | ✓ | ✓ | | | | | | | | ✓ | | ✓ |

Figure 2–73 shows the global and regional clocking from enhanced PLL outputs and top and bottom CLK pins.

Figure 2–73. Global and Regional Clock Connections from Top and Bottom Clock Pins and Enhanced PLL Outputs Notes (1), (2)



Notes to Figure 2–73:

- (1) EP2SGX30C/D and EP2SGX60C/D devices only have two enhanced PLLs (5 and 6), but the connectivity from these two PLLs to the global and regional clock networks remains the same as shown.
- (2) If the design uses the feedback input, you will lose one (or two, if FBIN is differential) external clock output pin.

The connections to the global and regional clocks from the top clock pins and enhanced PLL outputs are shown in Table 2–28. The connections to the clocks from the bottom clock pins are shown in Table 2–29.

Table 2–28. Global and Regional Clock Connections from Top Clock Pins and Enhanced PLL Outputs (Part 1 of 2)

| Top Side Global and Regional Clock Network Connectivity | DLLCLK | CLK12 | CLK13 | CLK14 | CLK15 | RCLK24 | RCLK25 | RCLK26 | RCLK27 | RCLK28 | RCLK29 | RCLK30 | RCLK31 |
|---|--------|-------|-------|-------|-------|--------|--------|--------|--------|--------|--------|--------|--------|
| Clock pins | | | | | | | | | | | | | |
| CLK12p | ✓ | ✓ | ✓ | | | ✓ | | | | ✓ | | | |
| CLK13p | ✓ | ✓ | ✓ | | | | ✓ | | | | ✓ | | |
| CLK14p | ✓ | | | ✓ | ✓ | | | ✓ | | | | ✓ | |
| CLK15p | ✓ | | | ✓ | ✓ | | | | ✓ | | | | ✓ |
| CLK12n | | ✓ | | | | ✓ | | | | ✓ | | | |
| CLK13n | | | ✓ | | | | ✓ | | | | ✓ | | |
| CLK14n | | | | ✓ | | | | ✓ | | | | ✓ | |
| CLK15n | | | | | ✓ | | | | ✓ | | | | ✓ |
| Drivers from internal logic | | | | | | | | | | | | | |
| GCLKDRV0 | | ✓ | | | | | | | | | | | |
| GCLKDRV1 | | | ✓ | | | | | | | | | | |
| GCLKDRV2 | | | | ✓ | | | | | | | | | |
| GCLKDRV3 | | | | | ✓ | | | | | | | | |
| RCLKDRV0 | | | | | | ✓ | | | | ✓ | | | |
| RCLKDRV1 | | | | | | | ✓ | | | | ✓ | | |
| RCLKDRV2 | | | | | | | | ✓ | | | | ✓ | |
| RCLKDRV3 | | | | | | | | | ✓ | | | | ✓ |
| RCLKDRV4 | | | | | | ✓ | | | | ✓ | | | |
| RCLKDRV5 | | | | | | | ✓ | | | | ✓ | | |
| RCLKDRV6 | | | | | | | | ✓ | | | | ✓ | |
| RCLKDRV7 | | | | | | | | | ✓ | | | | ✓ |
| Enhanced PLL5 outputs | | | | | | | | | | | | | |
| c0 | ✓ | ✓ | ✓ | | | ✓ | | | | ✓ | | | |
| c1 | ✓ | ✓ | ✓ | | | | ✓ | | | | ✓ | | |

Table 2–28. Global and Regional Clock Connections from Top Clock Pins and Enhanced PLL Outputs (Part 2 of 2)

| Top Side Global and Regional Clock Network Connectivity | DLLCLK | CLK12 | CLK13 | CLK14 | CLK15 | RCLK24 | RCLK25 | RCLK26 | RCLK27 | RCLK28 | RCLK29 | RCLK30 | RCLK31 |
|---|--------|-------|-------|-------|-------|--------|--------|--------|--------|--------|--------|--------|--------|
| c2 | ✓ | | | ✓ | ✓ | | | ✓ | | | | ✓ | |
| c3 | ✓ | | | ✓ | ✓ | | | | ✓ | | | | ✓ |
| c4 | ✓ | | | | | ✓ | | ✓ | | ✓ | | ✓ | |
| c5 | ✓ | | | | | | ✓ | | ✓ | | ✓ | | ✓ |
| Enhanced PLL 11 outputs | | | | | | | | | | | | | |
| c0 | | ✓ | ✓ | | | ✓ | | | | ✓ | | | |
| c1 | | ✓ | ✓ | | | | ✓ | | | | ✓ | | |
| c2 | | | | ✓ | ✓ | | | ✓ | | | | ✓ | |
| c3 | | | | ✓ | ✓ | | | | ✓ | | | | ✓ |
| c4 | | | | | | ✓ | | ✓ | | ✓ | | ✓ | |
| c5 | | | | | | | ✓ | | ✓ | | ✓ | | ✓ |

Table 2–29. Global and Regional Clock Connections from Bottom Clock Pins and Enhanced PLL Outputs (Part 1 of 2)

| Bottom Side Global and Regional Clock Network Connectivity | DLLCLK | CLK4 | CLK5 | CLK6 | CLK7 | RCLK8 | RCLK9 | RCLK10 | RCLK11 | RCLK12 | RCLK13 | RCLK14 | RCLK15 |
|--|--------|------|------|------|------|-------|-------|--------|--------|--------|--------|--------|--------|
| Clock pins | | | | | | | | | | | | | |
| CLK4p | ✓ | ✓ | ✓ | | | ✓ | | | | ✓ | | | |
| CLK5p | ✓ | ✓ | ✓ | | | | ✓ | | | | ✓ | | |
| CLK6p | ✓ | | | ✓ | ✓ | | | ✓ | | | | ✓ | |
| CLK7p | ✓ | | | ✓ | ✓ | | | | ✓ | | | | ✓ |
| CLK4n | | ✓ | | | | ✓ | | | | ✓ | | | |
| CLK5n | | | ✓ | | | | ✓ | | | | ✓ | | |
| CLK6n | | | | ✓ | | | | ✓ | | | | ✓ | |
| CLK7n | | | | | ✓ | | | | ✓ | | | | ✓ |
| Drivers from internal logic | | | | | | | | | | | | | |
| GCLKDRV0 | | ✓ | | | | | | | | | | | |
| GCLKDRV1 | | | ✓ | | | | | | | | | | |

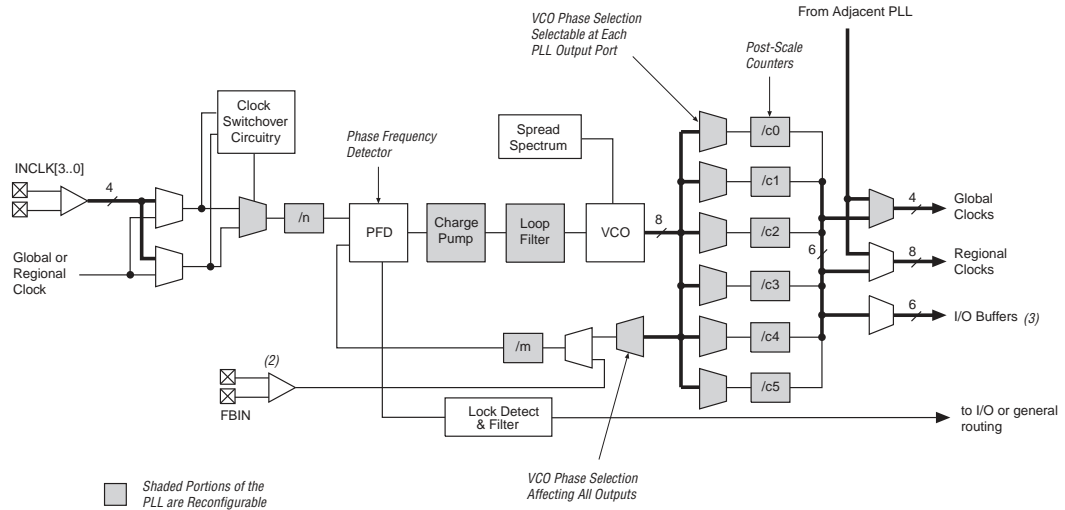
Table 2–29. Global and Regional Clock Connections from Bottom Clock Pins and Enhanced PLL Outputs (Part 2 of 2)

| Bottom Side Global and Regional Clock Network Connectivity | DLLCLK | CLK4 | CLK5 | CLK6 | CLK7 | RCLK8 | RCLK9 | RCLK10 | RCLK11 | RCLK12 | RCLK13 | RCLK14 | RCLK15 |
|--|--------|------|------|------|------|-------|-------|--------|--------|--------|--------|--------|--------|
| GCLKDRV2 | | | | ✓ | | | | | | | | | |
| GCLKDRV3 | | | | | ✓ | | | | | | | | |
| RCLKDRV0 | | | | | | ✓ | | | | ✓ | | | |
| RCLKDRV1 | | | | | | | ✓ | | | | ✓ | | |
| RCLKDRV2 | | | | | | | | ✓ | | | | ✓ | |
| RCLKDRV3 | | | | | | | | | ✓ | | | | ✓ |
| RCLKDRV4 | | | | | | ✓ | | | | ✓ | | | |
| RCLKDRV5 | | | | | | | ✓ | | | | ✓ | | |
| RCLKDRV6 | | | | | | | | ✓ | | | | ✓ | |
| RCLKDRV7 | | | | | | | | | ✓ | | | | ✓ |
| Enhanced PLL 6 outputs | | | | | | | | | | | | | |
| c0 | ✓ | ✓ | ✓ | | | ✓ | | | | ✓ | | | |
| c1 | ✓ | ✓ | ✓ | | | | ✓ | | | | ✓ | | |
| c2 | ✓ | | | ✓ | ✓ | | | ✓ | | | | ✓ | |
| c3 | ✓ | | | ✓ | ✓ | | | | ✓ | | | | ✓ |
| c4 | ✓ | | | | | ✓ | | ✓ | | ✓ | | ✓ | |
| c5 | ✓ | | | | | | ✓ | | ✓ | | ✓ | | ✓ |
| Enhanced PLL 12 outputs | | | | | | | | | | | | | |
| c0 | | ✓ | ✓ | | | ✓ | | | | ✓ | | | |
| c1 | | ✓ | ✓ | | | | ✓ | | | | ✓ | | |
| c2 | | | | ✓ | ✓ | | | ✓ | | | | ✓ | |
| c3 | | | | ✓ | ✓ | | | | ✓ | | | | ✓ |
| c4 | | | | | | ✓ | | ✓ | | ✓ | | ✓ | |
| c5 | | | | | | | ✓ | | ✓ | | ✓ | | ✓ |

Enhanced PLLs

Stratix II GX devices contain up to four enhanced PLLs with advanced clock management features. These features include support for external clock feedback mode, spread-spectrum clocking, and counter cascading. Figure 2-74 shows a diagram of the enhanced PLL.

Figure 2-74. Stratix II GX Enhanced PLL Note (1)

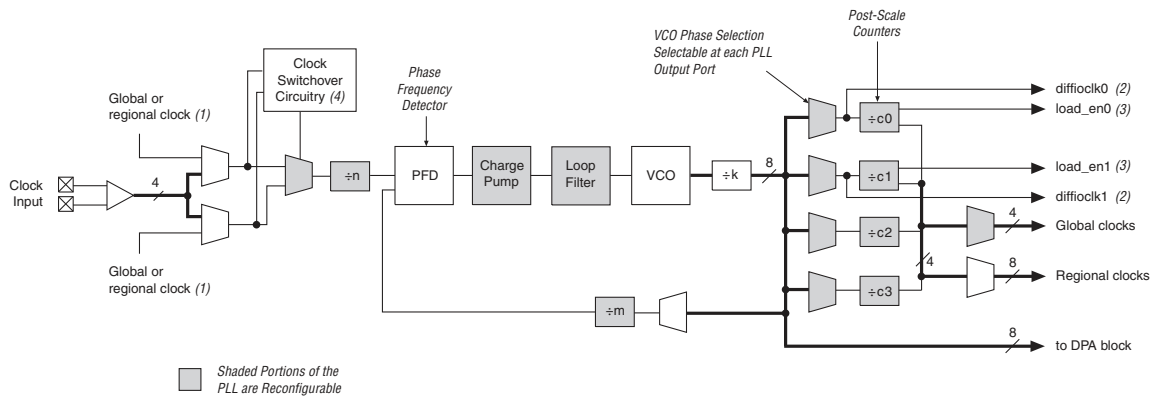


Notes to Figure 2-74:

- (1) Each clock source can come from any of the four clock pins that are physically located on the same side of the device as the PLL.
- (2) If the feedback input is used, you will lose one (or two, if FBIN is differential) external clock output pin.
- (3) Each enhanced PLL has three differential external clock outputs or six single-ended external clock outputs.
- (4) The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL.

Fast PLLs

Stratix II GX devices contain up to four fast PLLs with high-speed serial interfacing ability. The fast PLLs offer high-speed outputs to manage the high-speed differential I/O interfaces. Figure 2-75 shows a diagram of the fast PLL.

Figure 2–75. Stratix II GX Device Fast PLL**Notes to Figure 2–75:**

- (1) The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL.
- (2) In high-speed differential I/O support mode, this high-speed PLL clock feeds the serializer/deserializer (SERDES) circuitry. Stratix II GX devices only support one rate of data transfer per fast PLL in high-speed differential I/O support mode.
- (3) This signal is a differential I/O SERDES control signal.
- (4) Stratix II GX fast PLLs only support manual clock switchover.



Refer to the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook* for more information on enhanced and fast PLLs. Refer to “[High-Speed Differential I/O with DPA Support](#)” on [page 2–136](#) for more information on high-speed differential I/O support.

I/O Structure

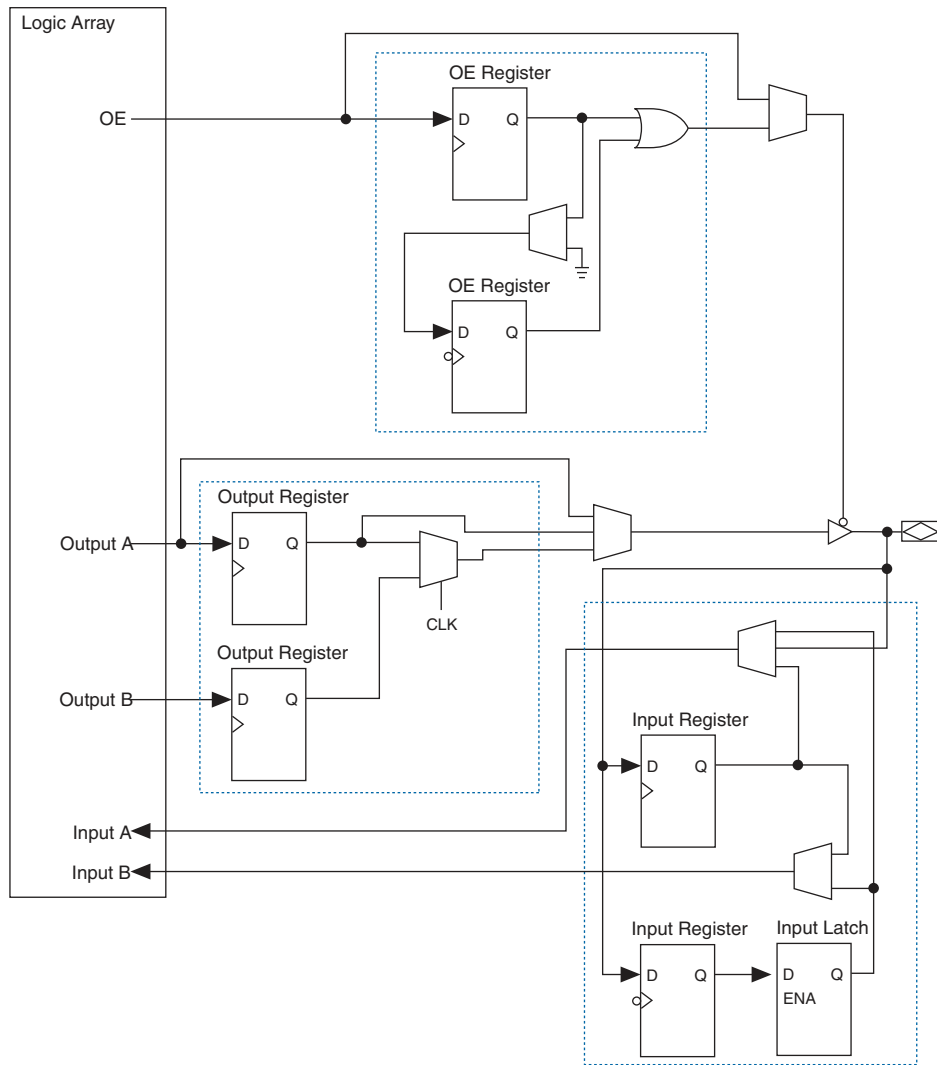
The Stratix II GX IOEs provide many features, including:

- Dedicated differential and single-ended I/O buffers
- 3.3-V, 64-bit, 66-MHz PCI compliance
- 3.3-V, 64-bit, 133-MHz PCI-X 1.0 compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- On-chip driver series termination
- On-chip termination for differential standards
- Programmable pull-up during configuration
- Output drive strength control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors
- Programmable input and output delays

- Open-drain outputs
- DQ and DQS I/O pins
- Double data rate (DDR) registers

The IOE in Stratix II GX devices contains a bidirectional I/O buffer, six registers, and a latch for a complete embedded bidirectional single data rate or DDR transfer. [Figure 2-76](#) shows the Stratix II GX IOE structure. The IOE contains two input registers (plus a latch), two output registers, and two output enable registers. You can use both input registers and the latch to capture DDR input and both output registers to drive DDR outputs. Additionally, you can use the output enable (OE) register for fast clock-to-output enable timing. The negative edge-clocked OE register is used for DDR SDRAM interfacing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins.

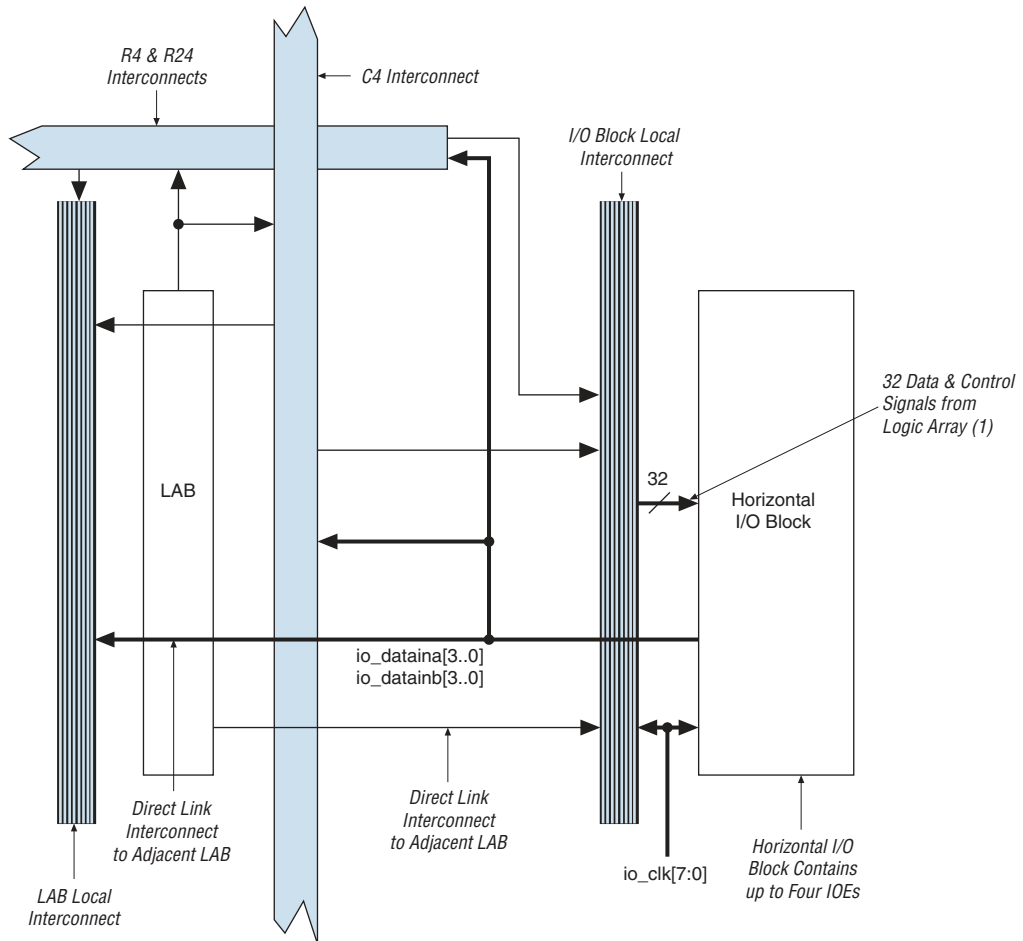
Figure 2-76. Stratix II GX IOE Structure



The IOEs are located in I/O blocks around the periphery of the Stratix II GX device. There are up to four IOEs per I/O block and four IOEs per column I/O block. The row I/O blocks drive row, column, or direct link interconnects. The column I/O blocks drive column interconnects.

Figure 2-77 shows how a row I/O block connects to the logic array.

Figure 2-77. Row I/O Block Connection to the Interconnect

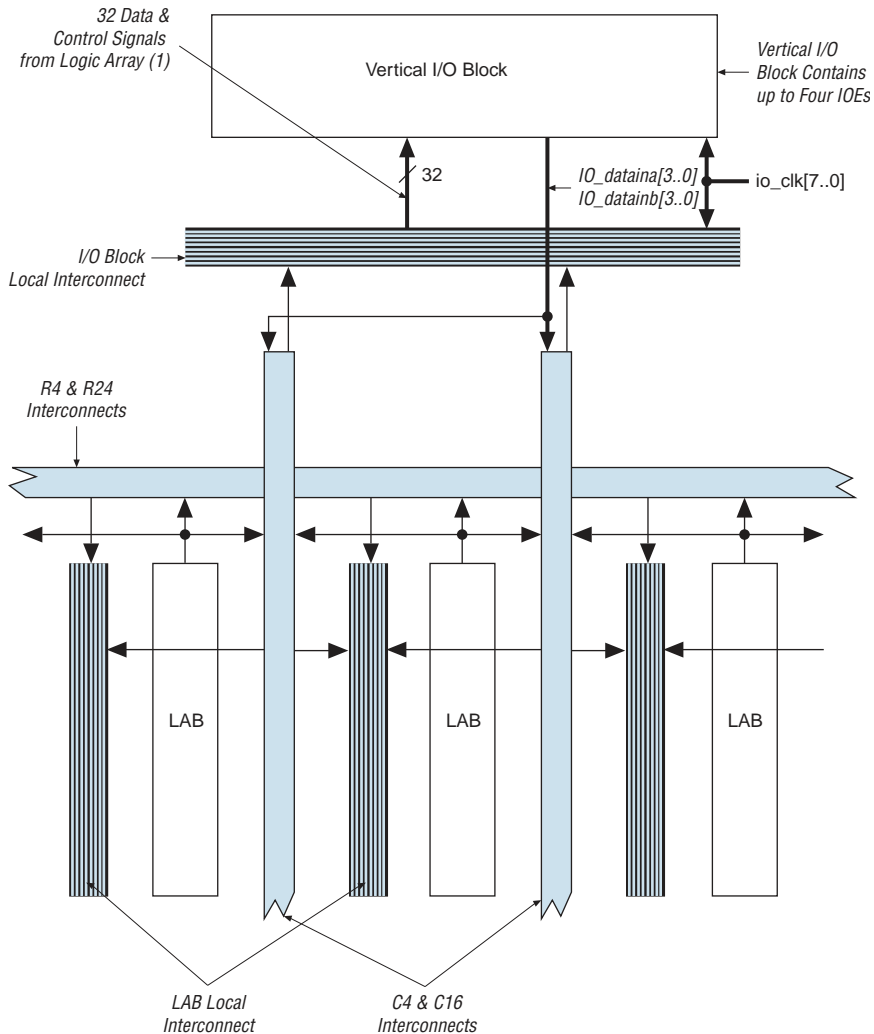


Note to Figure 2-77:

- (1) The 32 data and control signals consist of eight data out lines: four lines each for DDR applications $io_dataouta[3..0]$ and $io_dataoutb[3..0]$, four output enables $io_oe[3..0]$, four input clock enables $io_ce_in[3..0]$, four output clock enables $io_ce_out[3..0]$, four clocks $io_clk[3..0]$, four asynchronous clear and preset signals $io_aclr/apreset[3..0]$, and four synchronous clear and preset signals $io_sclr/spreset[3..0]$.

Figure 2–78 shows how a column I/O block connects to the logic array.

Figure 2–78. Column I/O Block Connection to the Interconnect



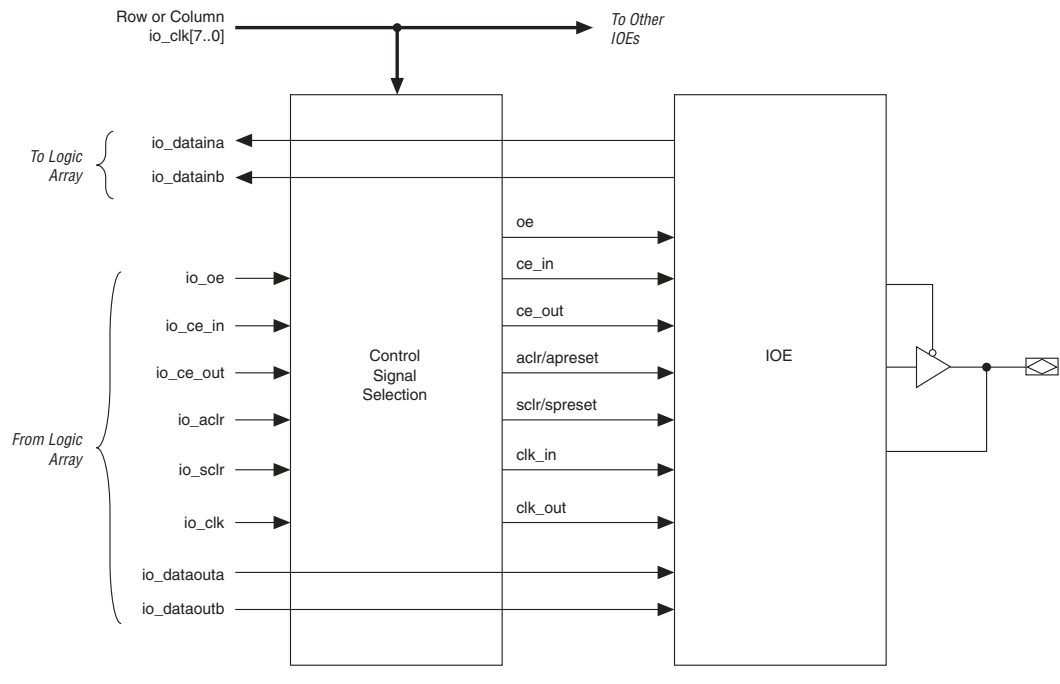
Note to Figure 2–78:

- (1) The 32 data and control signals consist of eight data out lines: four lines each for DDR applications $io_dataouta[3..0]$ and $io_dataoutb[3..0]$, four output enables $io_oe[3..0]$, four input clock enables $io_ce_in[3..0]$, four output clock enables $io_ce_out[3..0]$, four clocks $io_clk[3..0]$, four asynchronous clear and preset signals $io_aclr/apreset[3..0]$, and four synchronous clear and preset signals $io_sclr/spreset[3..0]$.

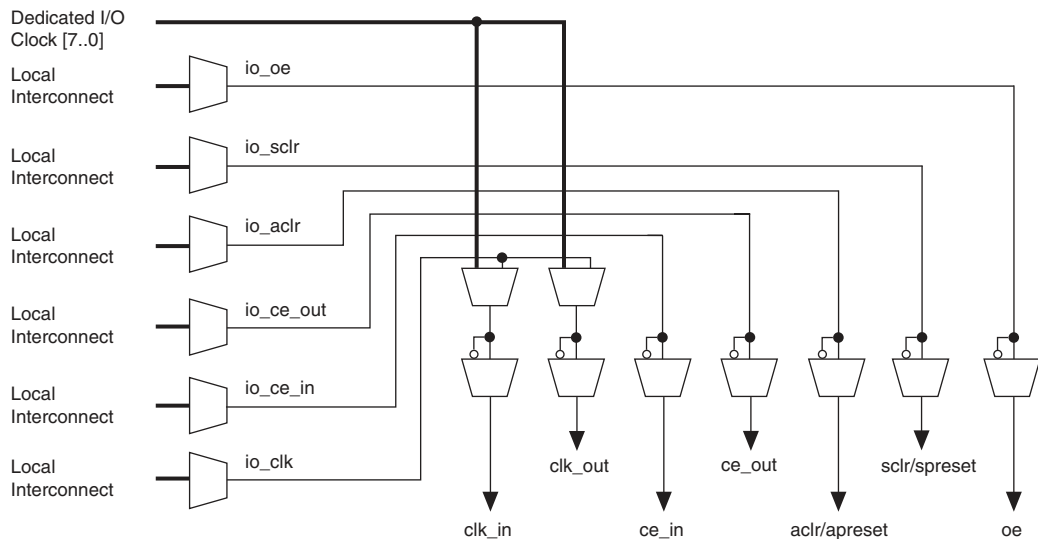
There are 32 control and data signals that feed each row or column I/O block. These control and data signals are driven from the logic array. The row or column IOE clocks, $io_clk[7..0]$, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from global or regional clocks. Refer to “PLLs and Clock Networks” on page 2–89 for more information.

Figure 2–79 illustrates the signal paths through the I/O block.

Figure 2–79. Signal Path Through the I/O Block



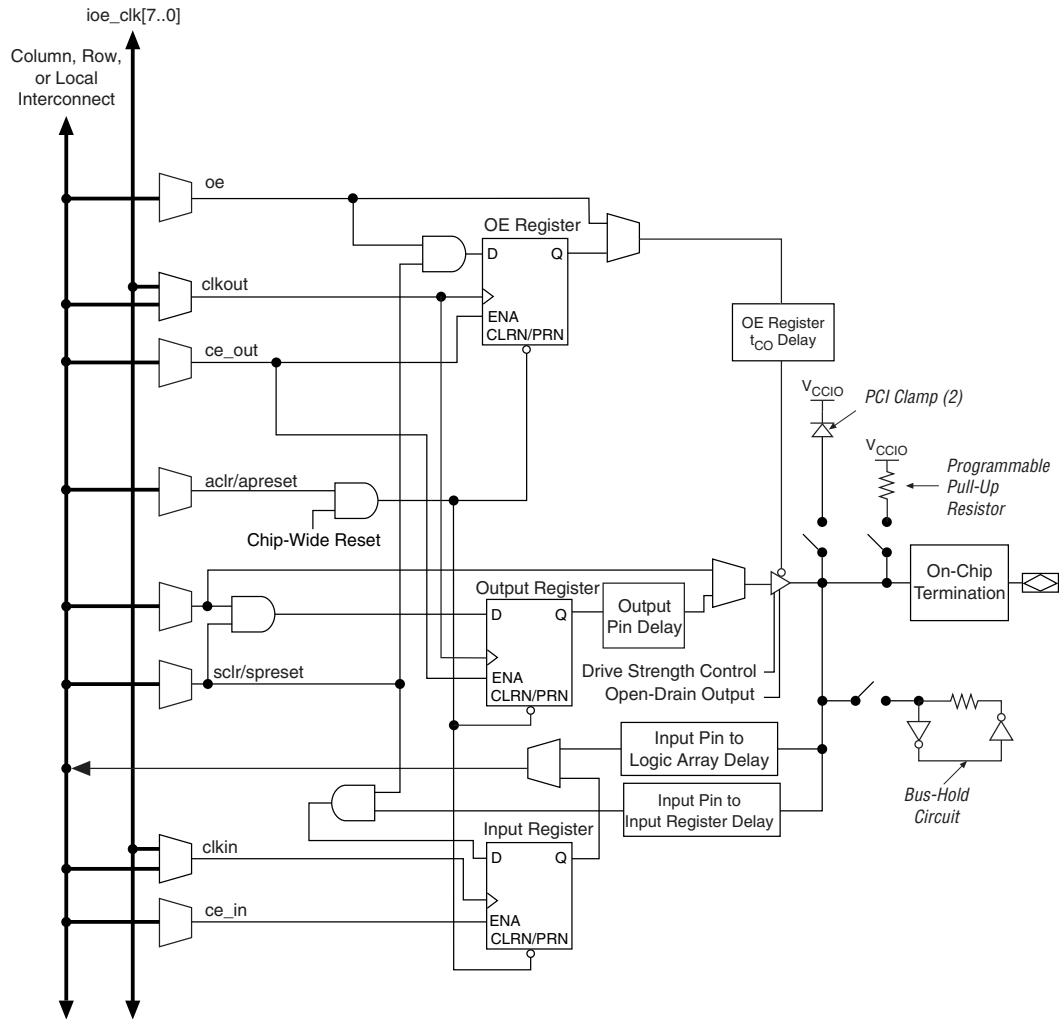
Each IOE contains its own control signal selection for the following control signals: oe , ce_in , ce_out , $aclr/apreset$, $sclr/spreset$, clk_in , and clk_out . Figure 2–80 illustrates the control signal selection.

Figure 2–80. Control Signal Selection per IOE *Note (1)***Note to Figure 2–80:**

- (1) Control signals `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, and `oe` can be global signals even though their control selection multiplexers are not directly fed by the `ioe_clk [7..0]` signals. The `ioe_clk` signals can drive the I/O local interconnect, which then drives the control selection multiplexers.

In normal bidirectional operation, you can use the input register for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. The output register can be used for data requiring fast clock-to-output performance. You can use the OE register for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from local interconnect in the associated LAB, dedicated I/O clocks, and the column and row interconnects. [Figure 2–81](#) shows the IOE in bidirectional configuration.

Figure 2–81. Stratix II GX IOE in Bidirectional I/O Configuration *Note (1)*



Notes to Figure 2–81:

- (1) All input signals to the IOE can be inverted at the IOE.
- (2) The optional PCI clamp is only available on column I/O pins.

The Stratix II GX device IOE includes programmable delays that can be activated to ensure input IOE register-to-logic array register transfers, input pin-to-logic array register transfers, or output IOE register-to-pin transfers.

A path in which a pin directly drives a register can require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinational logic may not require the delay. Programmable delays exist for decreasing input-pin-to-logic-array and IOE input register delays. The Quartus II Compiler can program these delays to automatically minimize setup time while providing a zero hold time. Programmable delays can increase the register-to-pin delays for output and/or output enable registers. Programmable delays are no longer required to ensure zero hold times for logic array register-to-IOE register transfers. The Quartus II Compiler can create the zero hold time for these transfers. [Table 2–30](#) shows the programmable delays for Stratix II GX devices.

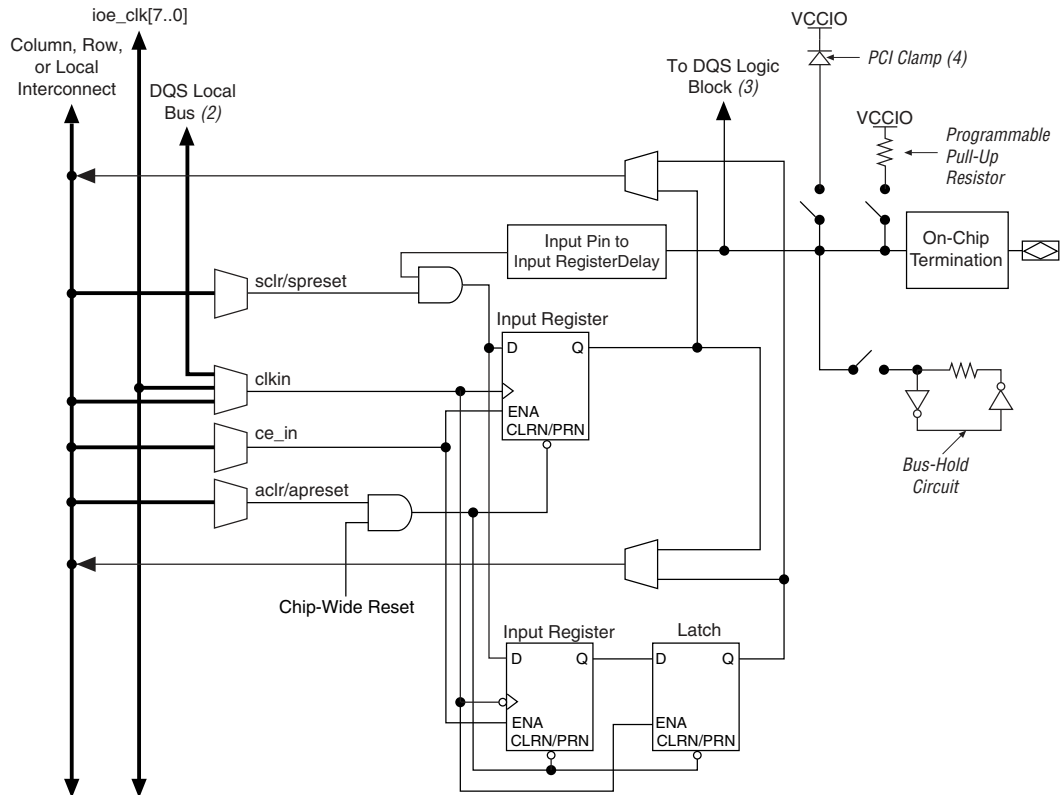
| Programmable Delays | Quartus II Logic Option |
|---------------------------------------|--|
| Input pin to logic array delay | Input delay from pin to internal cells |
| Input pin to input register delay | Input delay from pin to input register |
| Output pin delay | Delay from output register to output pin |
| Output enable register t_{CO} delay | Delay to output enable pin |

The IOE registers in Stratix II GX devices share the same source for clear or preset. You can program preset or clear for each individual IOE. You can also program the registers to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power-up. If one register in an IOE uses a preset or clear signal, all registers in the IOE must use that same signal if they require preset or clear. Additionally, a synchronous reset signal is available for the IOE registers.

Double Data Rate I/O Pins

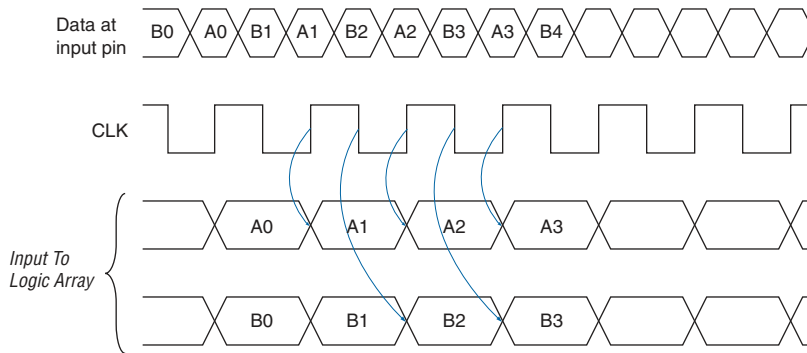
Stratix II GX devices have six registers in the IOE, which support DDR interfacing by clocking data on both positive and negative clock edges. The IOEs in Stratix II GX devices support DDR inputs, DDR outputs, and bidirectional DDR modes. When using the IOE for DDR inputs, the two input registers clock double rate input data on alternating edges. An input latch is also used in the IOE for DDR input acquisition. The latch holds the data that is present during the clock high times, allowing both bits of data to be synchronous with the same clock edge (either rising or falling). [Figure 2–82](#) shows an IOE configured for DDR input. [Figure 2–83](#) shows the DDR input timing diagram.

Figure 2–82. Stratix II GX IOE in DDR Input I/O Configuration *Note (1)*

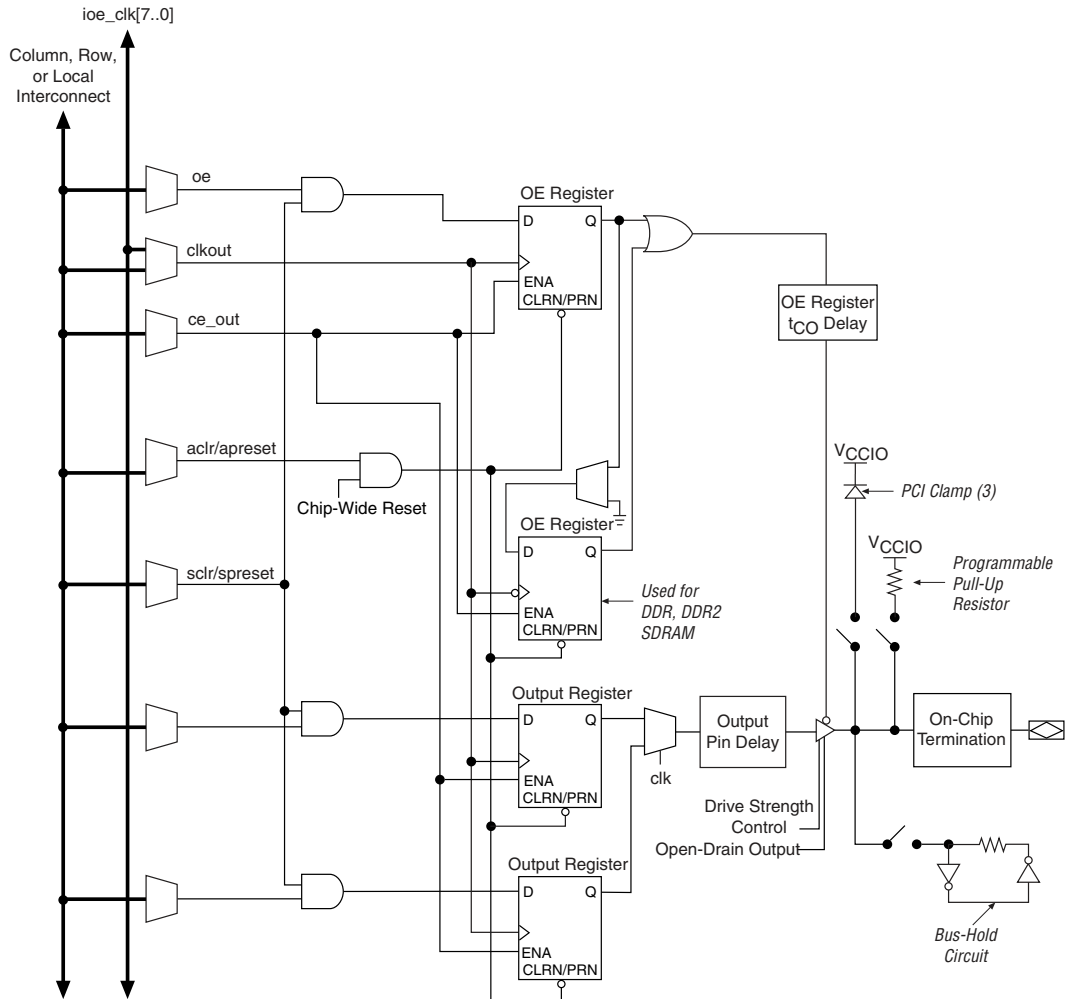


Notes to Figure 2–82:

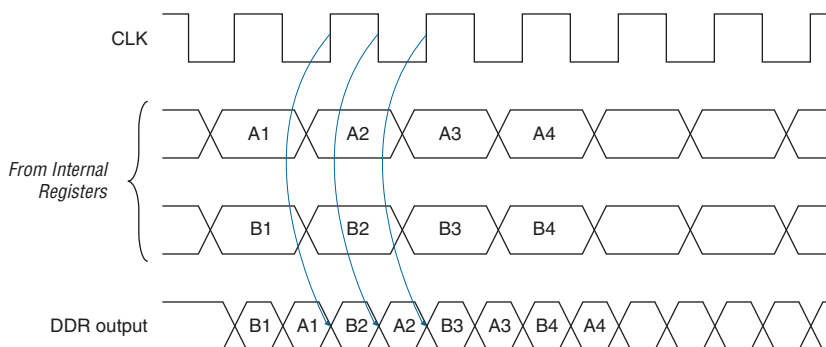
- (1) All input signals to the IOE can be inverted at the IOE.
- (2) This signal connection is only allowed on dedicated DQ function pins.
- (3) This signal is for dedicated DQS function pins only.
- (4) The optional PCI clamp is only available on column I/O pins.

Figure 2–83. Input Timing Diagram in DDR Mode

When using the IOE for DDR outputs, the two output registers are configured to clock two data paths from ALMs on rising clock edges. These output registers are multiplexed by the clock to drive the output pin at a $\times 2$ rate. One output register clocks the first bit out on the clock high time, while the other output register clocks the second bit out on the clock low time. [Figure 2–84](#) shows the IOE configured for DDR output. [Figure 2–85](#) shows the DDR output timing diagram.

Figure 2–84. Stratix II GX IOE in DDR Output I/O Configuration Notes (1), (2)

Notes to Figure 2–84:

- (1) All input signals to the IOE can be inverted at the IOE.
- (2) The tri-state buffer is active low. The DDIO megafunction represents the tri-state buffer as active-high with an inverter at the OE register data port.
- (3) The optional PCI clamp is only available on column I/O pins.

Figure 2–85. Output Timing Diagram in DDR Mode

The Stratix II GX IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations. The negative-edge-clocked OE register holds the OE signal inactive until the falling edge of the clock to meet DDR SDRAM timing requirements.

External RAM Interfacing

In addition to the six I/O registers in each IOE, Stratix II GX devices also have dedicated phase-shift circuitry for interfacing with external memory interfaces, including DDR and DDR2 SDRAM, QDR II SRAM, RLDRAM II, and SDR SDRAM. In every Stratix II GX device, the I/O banks at the top (banks 3 and 4) and bottom (banks 7 and 8) of the device support DQ and DQS signals with DQ bus modes of $\times 4$, $\times 8/\times 9$, $\times 16/\times 18$, or $\times 32/\times 36$. [Table 2–31](#) shows the number of DQ and DQS buses that are supported per device.

Table 2–31. DQS and DQ Bus Mode Support

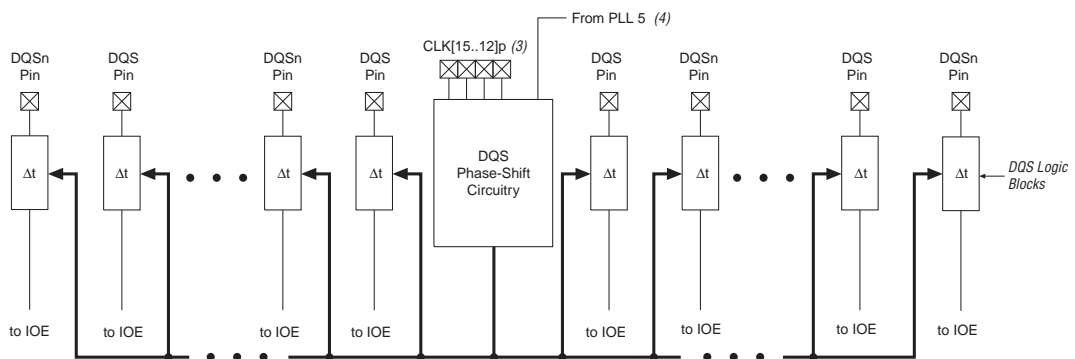
| Device | Package | Number of $\times 4$ Groups | Number of $\times 8/\times 9$ Groups | Number of $\times 16/\times 18$ Groups | Number of $\times 32/\times 36$ Groups |
|-----------|------------------------|-----------------------------|--------------------------------------|--|--|
| EP2SGX30 | 780-pin FineLine BGA | 18 | 8 | 4 | 0 |
| EP2SGX60 | 780-pin FineLine BGA | 18 | 8 | 4 | 0 |
| | 1,152-pin FineLine BGA | 36 | 18 | 8 | 4 |
| EP2SGX90 | 1,152-pin FineLine BGA | 36 | 18 | 8 | 4 |
| | 1,508-pin FineLine BGA | 36 | 18 | 8 | 4 |
| EP2SGX130 | 1,508-pin FineLine BGA | 36 | 18 | 8 | 4 |

A compensated delay element on each DQS pin automatically aligns input DQS synchronization signals with the data window of their corresponding DQ data signals. The DQS signals drive a local DQS bus in the top and bottom I/O banks. This DQS bus is an additional resource to the I/O clocks and is used to clock DQ input registers with the DQS signal.

The Stratix II GX device has two phase-shifting reference circuits, one on the top and one on the bottom of the device. The circuit on the top controls the compensated delay elements for all DQS pins on the top. The circuit on the bottom controls the compensated delay elements for all DQS pins on the bottom.

Each phase-shifting reference circuit is driven by a system reference clock, which must have the same frequency as the DQS signal. Clock pins $CLK[15..12]_p$ feed the phase circuitry on the top of the device and clock pins $CLK[7..4]_p$ feed the phase circuitry on the bottom of the device. In addition, PLL clock outputs can also feed the phase-shifting reference circuits. [Figure 2–86](#) shows the phase-shift reference circuit control of each DQS delay shift on the top of the device. This same circuit is duplicated on the bottom of the device.

Figure 2–86. DQS Phase-Shift Circuitry Notes (1), (2)



Notes to Figure 2–86:

- (1) There are up to 18 pairs of DQS and DQSn pins available on the top or the bottom of the Stratix II GX device. There are up to 10 pairs on the right side and 8 pairs on the left side of the DQS phase-shift circuitry.
- (2) The "t" module represents the DQS logic block.
- (3) Clock pins $CLK[15..12]_p$ feed the phase-shift circuitry on the top of the device and clock pins $CLK[7..4]_p$ feed the phase circuitry on the bottom of the device. You can also use a PLL clock output as a reference clock to the phaseshift circuitry.
- (4) You can only use PLL 5 to feed the DQS phase-shift circuitry on the top of the device and PLL 6 to feed the DQS phase-shift circuitry on the bottom of the device.

These dedicated circuits combined, with enhanced PLL clocking and phase-shift ability, provide a complete hardware solution for interfacing to high-speed memory.



For more information on external memory interfaces, refer to the *External Memory Interfaces in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*.

Programmable Drive Strength

The output buffer for each Stratix II GX device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTTL, LVCMOS, SSTL, and HSTL standards have several levels of drive strength that you can control. The default setting used in the Quartus II software is the maximum current strength setting that is used to achieve maximum I/O performance. For all I/O standards, the minimum setting is the lowest drive strength that guarantees the I_{OH}/I_{OL} of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.

Table 2–32 shows the possible settings for the I/O standards with drive strength control.

Table 2–32. Programmable Drive Strength *Note (1)*

| I/O Standard | I_{OH} / I_{OL} Current Strength Setting (mA) for Column I/O Pins | I_{OH} / I_{OL} Current Strength Setting (mA) for Row I/O Pins |
|---------------------|---|--|
| 3.3-V LVTTTL | 24, 20, 16, 12, 8, 4 | 12, 8, 4 |
| 3.3-V LVCMOS | 24, 20, 16, 12, 8, 4 | 8, 4 |
| 2.5-V LVTTTL/LVCMOS | 16, 12, 8, 4 | 12, 8, 4 |
| 1.8-V LVTTTL/LVCMOS | 12, 10, 8, 6, 4, 2 | 8, 6, 4, 2 |
| 1.5-V LVCMOS | 8, 6, 4, 2 | 4, 2 |
| SSTL-2 Class I | 12, 8 | 12, 8 |
| SSTL-2 Class II | 24, 20, 16 | 16 |
| SSTL-18 Class I | 12, 10, 8, 6, 4 | 10, 8, 6, 4 |
| SSTL-18 Class II | 20, 18, 16, 8 | — |
| HSTL-18 Class I | 12, 10, 8, 6, 4 | 12, 10, 8, 6, 4 |
| HSTL-18 Class II | 20, 18, 16 | — |
| HSTL-15 Class I | 12, 10, 8, 6, 4 | 8, 6, 4 |
| HSTL-15 Class II | 20, 18, 16 | — |

Note to Table 2–32:

- (1) The Quartus II software default current setting is the maximum setting for each I/O standard.

Open-Drain Output

Stratix II GX devices provide an optional open-drain (equivalent to an open collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (for example, interrupt and write enable signals) that can be asserted by any of several devices.

Bus Hold

Each Stratix II GX device I/O pin provides an optional bus-hold feature. The bus-hold circuitry can hold the signal on an I/O pin at its last-driven state. Since the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not needed to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than V_{CCIO} to prevent overdriving signals. If the bus-hold feature is enabled, the programmable pull-up option cannot be used. Disable the bus-hold feature when the I/O pin has been configured for differential signals.

The bus-hold circuitry uses a resistor with a nominal resistance (RBH) of approximately 7 k Ω to pull the signal level to the last-driven state.



Refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II GX Device Handbook* for the specific sustaining current driven through this resistor and overdrive current used to identify the next-driven input level. This information is provided for each V_{CCIO} voltage level.

The bus-hold circuitry is active only after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

Programmable Pull-Up Resistor

Each Stratix II GX device I/O pin provides an optional programmable pull-up resistor during user mode. If you enable this feature for an I/O pin, the pull-up resistor (typically 25 k Ω) holds the output to the V_{CCIO} level of the output pin's bank.

Programmable pull-up resistors are only supported on user I/O pins and are not supported on dedicated configuration pins, JTAG pins, or dedicated clock pins.

Advanced I/O Standard Support

The Stratix II GX device IOEs support the following I/O standards:

- 3.3-V LVTTTL/LVCMOS
- 2.5-V LVTTTL/LVCMOS
- 1.8-V LVTTTL/LVCMOS
- 1.5-V LVCMOS
- 3.3-V PCI
- 3.3-V PCI-X mode 1
- LVDS
- LVPECL (on input and output clocks only)
- Differential 1.5-V HSTL class I and II
- Differential 1.8-V HSTL class I and II
- Differential SSTL-18 class I and II

- Differential SSTL-2 class I and II
- 1.2-V HSTL class I and II
- 1.5-V HSTL class I and II
- 1.8-V HSTL class I and II
- SSTL-2 class I and II
- SSTL-18 class I and II

Table 2–33 describes the I/O standards supported by Stratix II GX devices.

| I/O Standard | Type | Input Reference Voltage (V_{REF}) (V) | Output Supply Voltage (V_{CCIO}) (V) | Board Termination Voltage (V_{TT}) (V) |
|--|--------------------|---|--|--|
| LVTTTL | Single-ended | — | 3.3 | — |
| LVCMOS | Single-ended | — | 3.3 | — |
| 2.5 V | Single-ended | — | 2.5 | — |
| 1.8 V | Single-ended | — | 1.8 | — |
| 1.5-V LVCMOS | Single-ended | — | 1.5 | — |
| 3.3-V PCI | Single-ended | — | 3.3 | — |
| 3.3-V PCI-X mode 1 | Single-ended | — | 3.3 | — |
| LVDS | Differential | — | 2.5 (3) | — |
| LVPECL (1) | Differential | — | 3.3 | — |
| HyperTransport technology | Differential | — | 2.5 (3) | — |
| Differential 1.5-V HSTL class I and II (2) | Differential | 0.75 | 1.5 | 0.75 |
| Differential 1.8-V HSTL class I and II (2) | Differential | 0.90 | 1.8 | 0.90 |
| Differential SSTL-18 class I and II (2) | Differential | 0.90 | 1.8 | 0.90 |
| Differential SSTL-2 class I and II (2) | Differential | 1.25 | 2.5 | 1.25 |
| 1.2-V HSTL(4) | Voltage-referenced | 0.6 | 1.2 | 0.6 |
| 1.5-V HSTL class I and II | Voltage-referenced | 0.75 | 1.5 | 0.75 |
| 1.8-V HSTL class I and II | Voltage-referenced | 0.9 | 1.8 | 0.9 |
| SSTL-18 class I and II | Voltage-referenced | 0.90 | 1.8 | 0.90 |

Table 2–33. Stratix II GX Supported I/O Standards

| I/O Standard | Type | Input Reference Voltage (V_{REF}) (V) | Output Supply Voltage (V_{CCIO}) (V) | Board Termination Voltage (V_{TT}) (V) |
|-----------------------|--------------------|---|--|--|
| SSTL-2 class I and II | Voltage-referenced | 1.25 | 2.5 | 1.25 |

Notes to Table 2–33:

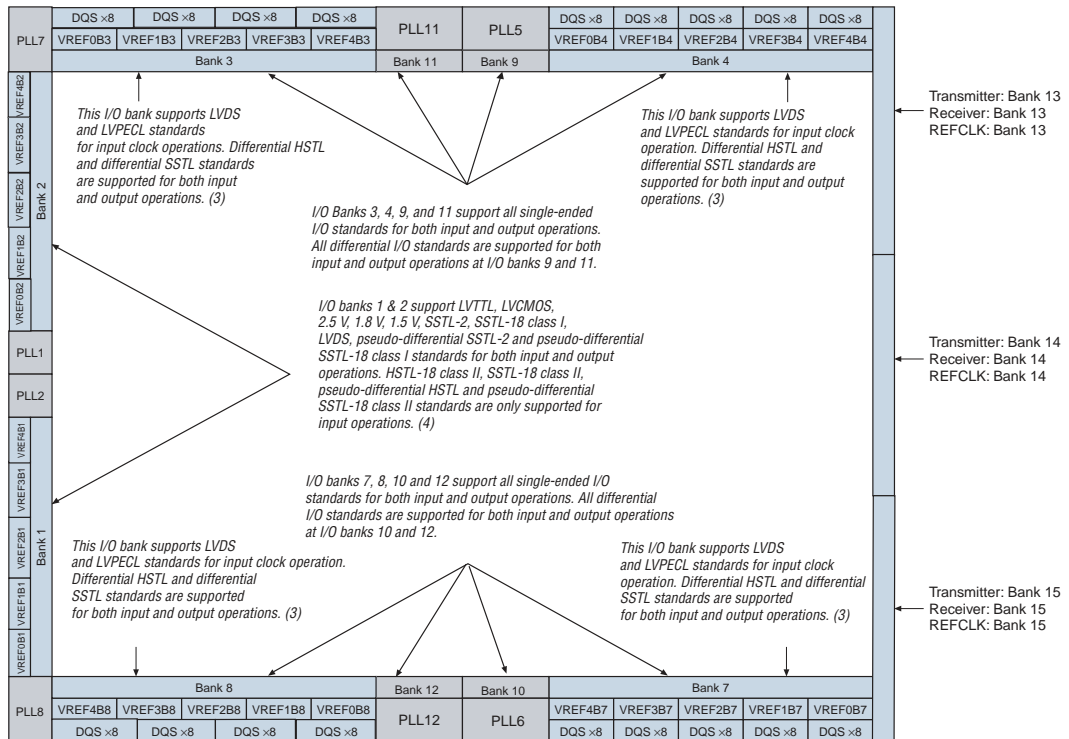
- (1) This I/O standard is only available on input and output column clock pins.
- (2) This I/O standard is only available on input clock pins and DQS pins in I/O banks 3, 4, 7, and 8, and output clock pins in I/O banks 9, 10, 11, and 12.
- (3) V_{CCIO} is 3.3 V when using this I/O standard in input and output column clock pins (in I/O banks 3, 4, 7, 8, 9, 10, 11, and 12).
- (4) 1.2-V HSTL is only supported in I/O banks 4, 7, and 8.



For more information on I/O standards supported by Stratix II GX I/O banks, refer to the *Selectable I/O Standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*.

Stratix II GX devices contain six I/O banks and four enhanced PLL external clock output banks, as shown in [Figure 2–87](#). The two I/O banks on the left of the device contain circuitry to support source-synchronous, high-speed differential I/O for LVDS inputs and outputs. These banks support all Stratix II GX I/O standards except PCI or PCI-X I/O pins, and SSTL-18 class II and HSTL outputs. The top and bottom I/O banks support all single-ended I/O standards. Additionally, enhanced PLL external clock output banks allow clock output capabilities such as differential support for SSTL and HSTL.

Figure 2–87. Stratix II GX I/O Banks Notes (1), (2)

**Notes to Figure 2–87:**

- Figure 2–87 is a top view of the silicon die that corresponds to a reverse view for flip-chip packages. It is a graphical representation only.
- Depending on the size of the device, different device members have different numbers of V_{REF} groups. Refer to the pin list and the Quartus II software for exact locations.
- Banks 9 through 12 are enhanced PLL external clock output banks.
- Horizontal I/O banks feature SERDES and DPA circuitry for high-speed differential I/O standards. See the *High-Speed Differential I/O Interfaces with DPA in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook 2* for more information on differential I/O standards.

Each I/O bank has its own V_{CCIO} pins. A single device can support 1.5-, 1.8-, 2.5-, and 3.3-V interfaces; each bank can support a different V_{CCIO} level independently. Each bank also has dedicated V_{REF} pins to support the voltage-referenced standards (such as SSTL-2).

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one V_{REF} voltage level. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTTL, LVCMOS, and 3.3-V PCI for inputs and outputs.

On-Chip Termination

Stratix II GX devices provide differential (for the LVDS technology I/O standard) and series on-chip termination to reduce reflections and maintain signal integrity. On-chip termination simplifies board design by minimizing the number of external termination resistors required. Termination can be placed inside the package, eliminating small stubs that can still lead to reflections.

Stratix II GX devices provide four types of termination:

- Differential termination (R_D)
- Series termination (R_S) without calibration
- Series termination (R_S) with calibration
- Parallel termination (R_T) with calibration

Table 2–34 shows the Stratix II GX on-chip termination support per I/O bank.

| On-Chip Termination Support | I/O Standard Support | Top and Bottom Banks (3, 4, 7, 8) | Left Bank (1, 2) |
|--|-----------------------|--------------------------------------|------------------|
| Series termination without calibration | 3.3-V LVTTTL | ✓ | ✓ |
| | 3.3-V LVCMOS | ✓ | ✓ |
| | 2.5-V LVTTTL | ✓ | ✓ |
| | 2.5-V LVCMOS | ✓ | ✓ |
| | 1.8-V LVTTTL | ✓ | ✓ |
| | 1.8-V LVCMOS | ✓ | ✓ |
| | 1.5-V LVTTTL | ✓ | ✓ |
| | 1.5-V LVCMOS | ✓ | ✓ |
| | SSTL-2 class I and II | ✓ | ✓ |
| | SSTL-18 class I | ✓ | ✓ |
| | SSTL-18 class II | ✓ | — |
| | 1.8-V HSTL class I | ✓ | ✓ |
| | 1.8-V HSTL class II | ✓ | — |
| | 1.5-V HSTL class I | ✓ | ✓ |
| | 1.2-V HSTL | ✓ | — |

Table 2–34. On-Chip Termination Support by I/O Banks (Part 2 of 2)

| On-Chip Termination Support | I/O Standard Support | Top and Bottom Banks (3, 4, 7, 8) | Left Bank (1, 2) |
|-------------------------------------|---------------------------|--------------------------------------|------------------|
| Series termination with calibration | 3.3-V LVTTTL | ✓ | — |
| | 3.3-V LVCMOS | ✓ | — |
| | 2.5-V LVTTTL | ✓ | — |
| | 2.5-V LVCMOS | ✓ | — |
| | 1.8-V LVTTTL | ✓ | — |
| | 1.8-V LVCMOS | ✓ | — |
| | 1.5-V LVTTTL | ✓ | — |
| | 1.5-V LVCMOS | ✓ | — |
| | SSTL-2 class I and II | ✓ | — |
| | SSTL-18 class I and II | ✓ | — |
| | 1.8-V HSTL class I | ✓ | — |
| | 1.8-V HSTL class II | ✓ | — |
| | 1.5-V HSTL class I | ✓ | — |
| 1.2-V HSTL | ✓ | — | |
| Differential termination (1) | LVDS | — | ✓ |
| | HyperTransport technology | — | ✓ |

Note to Table 2–34:

- (1) Clock pins CLK1 and CLK3, and pins FPLL [7 . . 8] CLK do not support differential on-chip termination. Clock pins CLK0 and CLK2, do support differential on-chip termination. Clock pins in the top and bottom banks (CLK [4 . . 7, 12 . . 15]) do not support differential on-chip termination.

Differential On-Chip Termination

Stratix II GX devices support internal differential termination with a nominal resistance value of 100 for LVDS input receiver buffers. LVPECL input signals (supported on clock pins only) require an external termination resistor. Differential on-chip termination is supported across the full range of supported differential data rates, as shown in the *High-Speed I/O Specifications* section of the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II GX Device Handbook*.



For more information on differential on-chip termination, refer to the *High-Speed Differential I/O Interfaces with DPA in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*.



For more information on tolerance specifications for differential on-chip termination, refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II GX Device Handbook*.

On-Chip Series Termination without Calibration

Stratix II GX devices support driver impedance matching to provide the I/O driver with controlled output impedance that closely matches the impedance of the transmission line. As a result, reflections can be significantly reduced. Stratix II GX devices support on-chip series termination for single-ended I/O standards with typical R_S values of 25 and 50 Ω . Once matching impedance is selected, current drive strength is no longer selectable. [Table 2–34](#) shows the list of output standards that support on-chip series termination without calibration.



For more information about series on-chip termination supported by Stratix II GX devices, refer to the *Selectable I/O Standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*.



For more information about tolerance specifications for on-chip termination without calibration, refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II GX Device Handbook*.

On-Chip Series Termination with Calibration

Stratix II GX devices support on-chip series termination with calibration in column I/O pins in top and bottom banks. There is one calibration circuit for the top I/O banks and one circuit for the bottom I/O banks. Each on-chip series termination calibration circuit compares the total impedance of each I/O buffer to the external 25- Ω or 50- Ω resistors connected to the RUP and RDN pins, and dynamically enables or disables the transistors until they match. Calibration occurs at the end of device configuration. Once the calibration circuit finds the correct impedance, it powers down and stops changing the characteristics of the drivers.



For more information about series on-chip termination supported by Stratix II GX devices, refer to the *Selectable I/O Standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*.



For more information about tolerance specifications for on-chip termination with calibration, refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II GX Device Handbook*.

On-Chip Parallel Termination with Calibration

Stratix II GX devices support on-chip parallel termination with calibration for column I/O pins only. There is one calibration circuit for the top I/O banks and one circuit for the bottom I/O banks. Each on-chip parallel termination calibration circuit compares the total impedance of each I/O buffer to the external 50- Ω resistors connected to the RUP and RDN pins and dynamically enables or disables the transistors until they match. Calibration occurs at the end of device configuration. Once the calibration circuit finds the correct impedance, it powers down and stops changing the characteristics of the drivers.



On-chip parallel termination with calibration is only supported for input pins.



For more information about on-chip termination supported by Stratix II devices, refer to the *Selectable I/O Standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*.



For more information about tolerance specifications for on-chip termination with calibration, refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II GX Device Handbook*.

MultiVolt I/O Interface

The Stratix II GX architecture supports the MultiVolt I/O interface feature that allows Stratix II GX devices in all packages to interface with systems of different supply voltages. The Stratix II GX VCCINT pins must always be connected to a 1.2-V power supply. With a 1.2-V VCCINT level, input pins are 1.2-, 1.5-, 1.8-, 2.5-, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.2-, 1.5-, 1.8-, 2.5-, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (for example, when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). The Stratix II GX VCCPD power pins must be connected to a 3.3-V power supply. These power pins are used to supply the pre-driver power to the output buffers, which increases the performance of the output pins. The VCCPD pins also power configuration input pins and JTAG input pins.

Table 2–35 summarizes Stratix II GX MultiVolt I/O support.

| V_{CCIO} (V) | Input Signal (V) | | | | | Output Signal (V) | | | | | |
|----------------|------------------|-------|-------|-------|-------|-------------------|-------|-------|-------|-----|-----|
| | 1.2 | 1.5 | 1.8 | 2.5 | 3.3 | 1.2 | 1.5 | 1.8 | 2.5 | 3.3 | 5.0 |
| 1.2 | (4) | ✓ (2) | ✓ (2) | ✓ (2) | ✓ (2) | ✓ (4) | — | — | — | — | — |
| 1.5 | (4) | ✓ | ✓ | ✓ (2) | ✓ (2) | ✓ (3) | ✓ | — | — | — | — |
| 1.8 | (4) | ✓ | ✓ | ✓ (2) | ✓ (2) | ✓ (3) | ✓ (3) | ✓ | — | — | — |
| 2.5 | (4) | — | — | ✓ | ✓ | ✓ (3) | ✓ (3) | ✓ (3) | ✓ | — | — |
| 3.3 | (4) | — | — | ✓ | ✓ | ✓ (3) | ✓ (3) | ✓ (3) | ✓ (3) | ✓ | ✓ |

Notes to Table 2–35:

- (1) To drive inputs higher than V_{CCIO} but less than 4.0 V, disable the PCI clamping diode and select the **Allow LVTTTL and LVC MOS input levels to overdrive input buffer** option in the Quartus II software.
- (2) The pin current may be slightly higher than the default value. You must verify that the driving device's V_{OL} maximum and V_{OH} minimum voltages do not violate the applicable Stratix II GX V_{IL} maximum and V_{IH} minimum voltage specifications.
- (3) Although V_{CCIO} specifies the voltage necessary for the Stratix II GX device to drive out, a receiving device powered at a different level can still interface with the Stratix II GX device if it has inputs that tolerate the V_{CCIO} value.
- (4) Stratix II GX devices support 1.2-V HSTL. They do not support 1.2-V LVTTTL and 1.2-V LVC MOS.

The TDO and nCEO pins are powered by V_{CCIO} of the bank that they reside. TDO is in I/O bank 4 and nCEO is in I/O bank 7. Ideally, the V_{CC} supplies for the I/O buffers of any two connected pins are at the same voltage level. This may not always be possible depending on the V_{CCIO} level of TDO and nCEO pins on master devices and the configuration voltage level chosen by V_{CCSEL} on slave devices. Master and slave devices can be in any position in the chain. Master indicates that it is driving out TDO or nCEO to a slave device. For multi-device passive configuration schemes, the nCEO pin of the master device drives the nCE pin of the slave device. The V_{CCSEL} pin on the slave device selects which input buffer is used for nCE. When V_{CCSEL} is logic high, it selects the 1.8-V/1.5-V buffer powered by V_{CCIO} . When V_{CCSEL} is logic low, it selects the 3.3-V/2.5-V input buffer powered by V_{CCPD} . The ideal case is to have the V_{CCIO} of the nCEO bank in a master device match the V_{CCSEL} settings for the nCE input buffer of the slave device it is connected to, but that may not be possible depending on the application.

Table 2–36 contains board design recommendations to ensure that nCEO can successfully drive nCE for all power supply combinations.

| nCE Input Buffer Power in I/O Bank 3 | Stratix II GX nCEO V_{CCIO} Voltage Level in I/O Bank 7 | | | | |
|--|---|---------------------------|---------------------------|---------------------------|---------------------------|
| | $V_{CCIO} = 3.3\text{ V}$ | $V_{CCIO} = 2.5\text{ V}$ | $V_{CCIO} = 1.8\text{ V}$ | $V_{CCIO} = 1.5\text{ V}$ | $V_{CCIO} = 1.2\text{ V}$ |
| VCCSEL high (V_{CCIO} Bank 3 = 1.5 V) | ✓ (1), (2) | ✓ (3), (4) | ✓ (5) | ✓ | ✓ |
| VCCSEL high (V_{CCIO} Bank 3 = 1.8 V) | ✓ (1), (2) | ✓ (3), (4) | ✓ | ✓ | Level shifter required |
| VCCSEL low (nCE powered by $V_{CCPD} = 3.3\text{ V}$) | ✓ | ✓ (4) | ✓ (6) | Level shifter required | Level shifter required |

Notes to Table 2–36:

- (1) Input buffer is 3.3-V tolerant.
- (2) The nCEO output buffer meets V_{OH} (MIN) = 2.4 V.
- (3) Input buffer is 2.5-V tolerant.
- (4) The nCEO output buffer meets V_{OH} (MIN) = 2.0 V.
- (5) Input buffer is 1.8-V tolerant.
- (6) An external 250- Ω pull-up resistor is not required, but recommended if signal levels on the board are not optimal.

For JTAG chains, the TDO pin of the first device drives the TDI pin of the second device in the chain. The V_{CCSEL} input on the JTAG input I/O cells (TCK, TMS, TDI, and TRST) is internally hardwired to GND selecting the 3.3-V/2.5-V input buffer powered by V_{CCPD} . The ideal case is to have the V_{CCIO} of the TDO bank from the first device match the V_{CCSEL} settings for TDI on the second device, but that may not be possible depending on the application. Table 2–37 contains board design recommendations to ensure proper JTAG chain operation.

| Device | TDI Input Buffer Power | Stratix II GX TDO V_{CCIO} Voltage Level in I/O Bank 4 | | | | |
|---------------|---------------------------|--|---------------------------|---------------------------|---------------------------|---------------------------|
| | | $V_{CCIO} = 3.3\text{ V}$ | $V_{CCIO} = 2.5\text{ V}$ | $V_{CCIO} = 1.8\text{ V}$ | $V_{CCIO} = 1.5\text{ V}$ | $V_{CCIO} = 1.2\text{ V}$ |
| Stratix II GX | Always V_{CCPD} (3.3 V) | ✓ (1) | ✓ (2) | ✓ (3) | Level shifter required | Level shifter required |

Table 2–37. Supported TDO/TDI Voltage Combinations (Part 2 of 2)

| Device | TDI Input Buffer Power | Stratix II GX TDO V_{CCIO} Voltage Level in I/O Bank 4 | | | | |
|-------------------|------------------------|--|---------------------------|---------------------------|---------------------------|---------------------------|
| | | $V_{CCIO} = 3.3\text{ V}$ | $V_{CCIO} = 2.5\text{ V}$ | $V_{CCIO} = 1.8\text{ V}$ | $V_{CCIO} = 1.5\text{ V}$ | $V_{CCIO} = 1.2\text{ V}$ |
| Non-Stratix II GX | VCC = 3.3 V | ✓ (1) | ✓ (2) | ✓ (3) | Level shifter required | Level shifter required |
| | VCC = 2.5 V | ✓ (1), (4) | ✓ (2) | ✓ (3) | Level shifter required | Level shifter required |
| | VCC = 1.8 V | ✓ (1), (4) | ✓ (2), (5) | ✓ | Level shifter required | Level shifter required |
| | VCC = 1.5 V | ✓ (1), (4) | ✓ (2), (5) | ✓ (6) | ✓ | ✓ |

Notes to Table 2–37:

- (1) The TDO output buffer meets $V_{OH}(\text{MIN}) = 2.4\text{ V}$.
- (2) The TDO output buffer meets $V_{OH}(\text{MIN}) = 2.0\text{ V}$.
- (3) An external 250- Ω pull-up resistor is not required, but recommended if signal levels on the board are not optimal.
- (4) Input buffer must be 3.3-V tolerant.
- (5) Input buffer must be 2.5-V tolerant.
- (6) Input buffer must be 1.8-V tolerant.

High-Speed Differential I/O with DPA Support

Stratix II GX devices contain dedicated circuitry for supporting differential standards at speeds up to 1 Gbps. The LVDS differential I/O standards are supported in the Stratix II GX device. In addition, the LVPECL I/O standard is supported on input and output clock pins on the top and bottom I/O banks.

The high-speed differential I/O circuitry supports the following high-speed I/O interconnect standards and applications:

- SPI-4 Phase 2 (POS-PHY Level 4)
- SFI-4
- Parallel RapidIO standard

There are two dedicated high-speed PLLs in the EP2SGX30 device and four dedicated high-speed PLLs in the EP2SGX60, EP2SGX90, and EP2SGX130 devices to multiply reference clocks and drive high-speed differential SERDES channels.

Tables 2–38 through 2–41 show the number of channels that each Fast PLL can clock in each of the Stratix II GX devices. In Tables 2–38 through 2–41, the first row for each transmitter or receiver provides the number of channels driven directly by the PLL. The second row below it shows the maximum channels a Fast PLL can drive if cross bank channels are used from the adjacent center Fast PLL. For example, in the 780-pin FineLine BGA EP2SGX30 device, PLL 1 can drive a maximum of

16 transmitter channels in I/O bank 1 or a maximum of 29 transmitter channels in I/O banks 1 and 2. The Quartus II software can also merge receiver and transmitter PLLs when a receiver is driving a transmitter. In this case, one fast PLL can drive both the maximum numbers of receiver and transmitter channels.

Table 2–38. EP2SGX30 Device Differential Channels *Note (1)*

| Package | Transmitter/Receiver | Total Channels | Center Fast PLLs Package | |
|----------------------|----------------------|----------------|--------------------------|------|
| | | | PLL1 | PLL2 |
| 780-pin FineLine BGA | Transmitter | 29 | 16 | 13 |
| | Receiver | 31 | 17 | 14 |

Table 2–39. EP2SGX60 Device Differential Channels *Note (1)*

| Package | Transmitter/Receiver | Total Channels | Center Fast PLLs | | Corner Fast PLLs | |
|------------------------|----------------------|----------------|------------------|------|------------------|------|
| | | | PLL1 | PLL2 | PLL7 | PLL8 |
| 780-pin FineLine BGA | Transmitter | 29 | 16 | 13 | — | — |
| | Receiver | 31 | 17 | 14 | — | — |
| 1,152-pin FineLine BGA | Transmitter | 42 | 21 | 21 | 21 | 21 |
| | Receiver | 42 | 21 | 21 | 21 | 21 |

Table 2–40. EP2SGX90 Device Differential Channels *Note (1)*

| Package | Transmitter/Receiver | Total Channels | Center Fast PLLs | | Corner Fast PLLs | |
|------------------------|----------------------|----------------|------------------|------|------------------|------|
| | | | PLL1 | PLL2 | PLL7 | PLL8 |
| 1,152-pin FineLine BGA | Transmitter | 45 | 23 | 22 | 23 | 22 |
| | Receiver | 47 | 23 | 24 | 23 | 24 |
| 1,508-pin FineLine BGA | Transmitter | 59 | 30 | 29 | 29 | 29 |
| | Receiver | 59 | 30 | 29 | 29 | 29 |

Table 2–41. EP2SGX130 Device Differential Channels *Note (1)*

| Package | Transmitter/Receiver | Total Channels | Center Fast PLLs | | Corner Fast PLLs | |
|-----------------------|----------------------|----------------|------------------|------|------------------|------|
| | | | PLL1 | PLL2 | PLL7 | PLL8 |
| 1508-pin FineLine BGA | Transmitter | 71 | 37 | 41 | 37 | 41 |
| | Receiver | 73 | 37 | 41 | 37 | 41 |

Note to Tables 2–38 through 2–41:

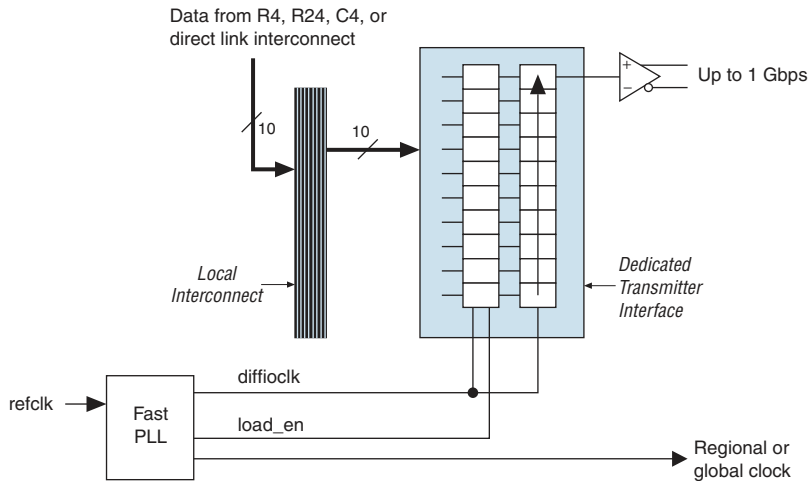
- (1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.

Therefore, the total number of channels is not the addition of the number of channels accessible by PLLs 1 and 2 with the number of channels accessible by PLLs 7 and 8.

Dedicated Circuitry with DPA Support

Stratix II GX devices support source-synchronous interfacing with LVDS signaling at up to 1 Gbps. Stratix II GX devices can transmit or receive serial channels along with a low-speed or high-speed clock.

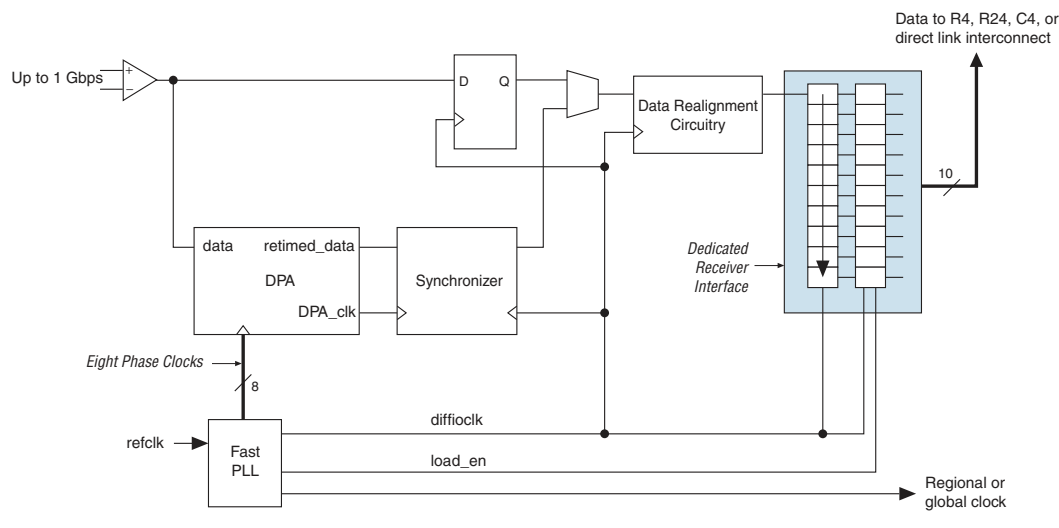
The receiving device PLL multiplies the clock by an integer factor $W = 1$ through 32. The SERDES factor J determines the parallel data width to deserialize from receivers or to serialize for transmitters. The SERDES factor J can be set to 4, 5, 6, 7, 8, 9, or 10 and does not have to equal the PLL clock-multiplication W value. A design using the dynamic phase aligner also supports all of these J factor values. For a J factor of 1, the Stratix II GX device bypasses the SERDES block. For a J factor of 2, the Stratix II GX device bypasses the SERDES block, and the DDR input and output registers are used in the IOE. [Figure 2–88](#) shows the block diagram of the Stratix II GX transmitter channel.

Figure 2–88. Stratix II GX Transmitter Channel

Each Stratix II GX receiver channel features a DPA block for phase detection and selection, a SERDES, a synchronizer, and a data realigner circuit. You can bypass the dynamic phase aligner without affecting the basic source-synchronous operation of the channel. In addition, you can dynamically switch between using the DPA block or bypassing the block via a control signal from the logic array.

Figure 2–89 shows the block diagram of the Stratix II GX receiver channel.

Figure 2–89. Stratix II GX Receiver Channel



An external pin or global or regional clock can drive the fast PLLs, which can output up to three clocks: two multiplied high-speed clocks to drive the SERDES block and/or external pin, and a low-speed clock to drive the logic array. In addition, eight phase-shifted clocks from the VCO can feed to the DPA circuitry.



For more information on the fast PLL, see the [PLLs in Stratix II GX Devices](#) chapter in volume 2 of the *Stratix II GX Handbook*.

The eight phase-shifted clocks from the fast PLL feed to the DPA block. The DPA block selects the closest phase to the center of the serial data eye to sample the incoming data. This allows the source-synchronous circuitry to capture incoming data correctly regardless of the channel-to-channel or clock-to-channel skew. The DPA block locks to a phase closest to the serial data phase. The phase-aligned DPA clock is used to write the data into the synchronizer.

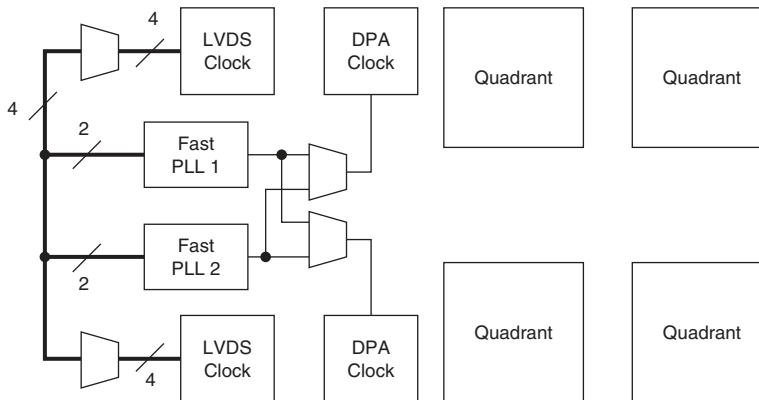
The synchronizer sits between the DPA block and the data realignment and SERDES circuitry. Since every channel utilizing the DPA block can have a different phase selected to sample the data, the synchronizer is needed to synchronize the data to the high-speed clock domain of the data realignment and the SERDES circuitry.

For high-speed source synchronous interfaces such as POS-PHY 4 and the Parallel RapidIO standard, the source synchronous clock rate is not a byte- or SERDES-rate multiple of the data rate. Byte alignment is necessary for these protocols because the source synchronous clock does not provide a byte or word boundary since the clock is one half the data rate, not one eighth. The Stratix II GX device's high-speed differential I/O circuitry provides dedicated data realignment circuitry for user-controlled byte boundary shifting. This simplifies designs while saving ALM resources. You can use an ALM-based state machine to signal the shift of receiver byte boundaries until a specified pattern is detected to indicate byte alignment.

Fast PLL and Channel Layout

The receiver and transmitter channels are interleaved such that each I/O bank on the left side of the device has one receiver channel and one transmitter channel per LAB row. [Figure 2-90](#) shows the fast PLL and channel layout in the EP2SGX30C/D and EP2SGX60C/D devices. [Figure 2-91](#) shows the fast PLL and channel layout in EP2SGX60E, EP2SGX90E/F, and EP2SGX130G devices.

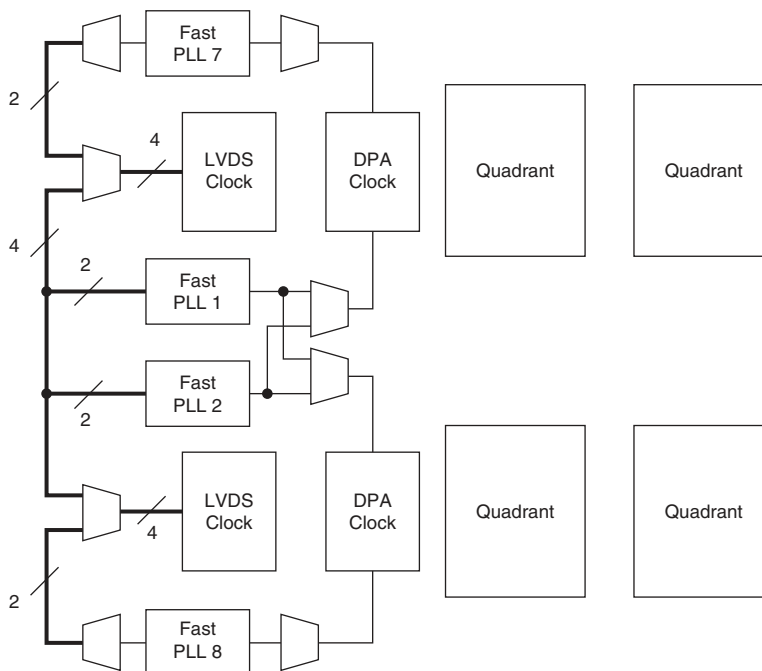
Figure 2-90. Fast PLL and Channel Layout in the EP2SGX30C/D and EP2SGX60C/D Devices *Note (1)*



Note to Figure 2-90:

(1) See [Table 2-38](#) for the number of channels each device supports.

Figure 2–91. Fast PLL and Channel Layout in the EP2SGX60E to EP2SGX130 Devices *Note (1)*



Note to Figure 2–91:

(1) See Tables 2–39 through Tables 2–41 for the number of channels each device supports.

Referenced Documents

This chapter references the following documents:

- *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II GX Handbook*
- *DSP Blocks in Stratix II GX Devices* chapter in Volume 2 of the *Stratix II GX Device Handbook*
- *External Memory Interfaces in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*
- *High-Speed Differential I/O Interfaces with DPA in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Handbook*
- *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*
- *Selectable I/O Standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Handbook*
- *Stratix II GX Device Handbook*, volume 2
- *Stratix II GX Transceiver Architecture Overview* chapter in volume 2 of the *Stratix II GX Handbook*

- *Stratix II Performance and Logic Efficiency Analysis White Paper*
- *TriMatrix Embedded Memory Blocks in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*

Document Revision History

Table 2–42 shows the revision history for this chapter.

| Table 2–42. Document Revision History (Part 1 of 6) | | |
|--|---|---------------------------|
| Date and Document Version | Changes Made | Summary of Changes |
| October 2007, v2.2 | Updated: <ul style="list-style-type: none"> ● “Programmable Pull-Up Resistor” ● “Reverse Serial Pre-CDR Loopback” ● “Receiver Input Buffer” ● “Pattern Detection” ● “Control and Status Signals” ● “Individual Power Down and Reset for the Transmitter and Receiver” | |
| | Updated: <ul style="list-style-type: none"> ● Figure 2–14 ● Figure 2–26 ● Figure 2–27 ● Figure 2–86 (notes only) ● Figure 2–87 | |
| | Updated: <ul style="list-style-type: none"> ● Table 2–4 ● Table 2–7 | |
| | Removed note from Table 2–31. | |
| | Removed Tables 2-2, 2-7, and 2-8. | |
| | Minor text edits. | |
| August 2007, v2.1 | Added “Reverse Serial Pre-CDR Loopback” section. | |
| | Updated Table 2–2. | |
| | Added “Referenced Documents” section. | |

| <i>Table 2–42. Document Revision History (Part 2 of 6)</i> | | |
|--|---|---|
| Date and Document Version | Changes Made | Summary of Changes |
| February 2007 v2.0 | Added Chapter 02 “Stratix II GX Transceivers” to the beginning of Chapter 03 “Stratix II GX Architecture”. <ul style="list-style-type: none"> • Changed chapter number to Chapter 02. | Combined Chapter 02 “Stratix II GX Transceivers” and Chapter 03 “Stratix II GX Architecture” in the new Chapter 02 “Stratix II GX Architecture” |
| | Added the “Document Revision History” section to this chapter. | |
| | Moved the “Stratix II GX Transceiver Clocking” section to after the “Receiver Path” section. | |

Table 2–42. Document Revision History (Part 3 of 6)

| Date and Document Version | Changes Made | Summary of Changes |
|---------------------------|---|--------------------|
| | Moved the “Transmit State Machine” section to after the “8B/10B Encoder” section. | |
| | Moved the “PCI Express Receiver Detect” and “PCI Express Electric Idles (or Individual Transmitter Tri-State)” sections to after the “Transmit Buffer” section. | |
| | Moved the “Dynamic Reconfiguration” section to the “Other Transceiver Features” section. | |
| | Moved the “Calibration Block”, “Receiver PLL & CRU”, and “Deserializer (Serial-to-Parallel Converter)” sections to the “Receiver Path” section. | |
| | Moved the “8B/10B Decoder” and “Receiver State Machine” sections to after the “Rate Matcher” section. | |
| | Moved the “Byte Ordering Block” section to after the “Byte Deserializer” section. | |
| | Updated the Clocking diagrams. | |
| | Added the “Clock Resource for PLD-Transceiver Interface” section. | |
| | Added the “On-Chip Parallel Termination with Calibration” section to the “On-Chip Termination” section. | |
| | Updated: <ul style="list-style-type: none"> ● Table 2–2. ● Table 2–10 ● Table 2–14. ● Table 2–3. ● Table 2–5. ● Table 2–8. ● Table 2–13 ● Table 2–18 ● Table 2–19 ● Table 2–29. | |
| | Updated Figures 2–3, 2–9, 2–24, 2–25, 2–28, 2–29, 2–60, 2–62. | |
| | Change 622 Mbps to 600 Mbps throughout the chapter. | |

| Table 2–42. Document Revision History (Part 4 of 6) | | |
|--|---|---------------------------|
| Date and Document Version | Changes Made | Summary of Changes |
| | Updated: <ul style="list-style-type: none"> ● “Transmitter PLLs” ● “Transmitter Phase Compensation FIFO Buffer” ● “8B/10B Encoder” ● “Byte Serializer” ● “Programmable Output Driver” ● “Receiver PLL & CRU” ● “Programmable Pre-Emphasis” ● “Receiver Input Buffer” ● “Control and Status Signals” ● “Programmable Run Length Violation” ● “Channel Aligner” ● “Basic Mode” ● “Byte Ordering Block” ● “Receiver Phase Compensation FIFO Buffer” ● “Loopback Modes” ● “Serial Loopback” ● “Parallel Loopback” ● “Regional Clock Network” ● “MultiVolt I/O Interface” ● “High-Speed Differential I/O with DPA Support” | |
| | Updated bulleted lists at the beginning of the “Transceivers” section. | |
| | Added reference to the “Transmit Buffer” section. | |
| | Deleted the Programmable V_{OD} table from the “Programmable Output Driver” section. | |
| | Changed “PLD Interface” heading to “Parallel Data Width” heading in Table 2–14. | |
| | Deleted “Global & Regional Clock Connections from Right Side Clock Pins & Fast PLL Outputs” table. | |
| | Updated notes to Tables 2–29 and 2–37. | |
| | Updated notes to Figures 2–72, 2–73 and 2–74. | |
| | Updated bulleted list in the “Advanced I/O Standard Support” section. | |

Table 2–42. Document Revision History (Part 5 of 6)

| Date and Document Version | Changes Made | Summary of Changes |
|---|--|---|
| <i>Previous Chapter 02 changes:</i> June 2006, v1.2 | <ul style="list-style-type: none"> ● Updated notes 1 and 2 in Figure 2–1. ● Updated “Byte Serializer” section. ● Updated Tables 2–4, 2–7, and 2–16. ● Updated “Programmable Output Driver” section. ● Updated Figure 2–12. ● Updated “Programmable Pre-Emphasis” section. ● Added Table 2–11. ● Added “Dynamic Reconfiguration” section. ● Added “Calibration Block” section. ● Updated “Programmable Equalizer” section, including addition of Figure 2–18. | Updated input frequency range in Table 2–4. |
| <i>Previous Chapter 02 changes:</i> April 2006, v1.1 | <ul style="list-style-type: none"> ● Updated Figure 2–3. ● Updated Figure 2–7. ● Updated Table 2–4. ● Updated “Transmit Buffer” section. | Updated input frequency range in Table 2–4. |
| <i>Previous Chapter 02 changes:</i> October 2005 v1.0 | Added chapter to the <i>Stratix II GX Device Handbook</i> . | |
| <i>Previous Chapter 03 changes:</i> August 2006, v1.4 | <ul style="list-style-type: none"> ● Updated Table 3–18 with note. | |
| <i>Previous Chapter 03 changes:</i> June 2006, v1.3 | <ul style="list-style-type: none"> ● Updated note 2 in Figure 3–41. ● Updated column title in Table 3–21. | |
| <i>Previous Chapter 03 changes:</i> April 2006, v1.2 | <ul style="list-style-type: none"> ● Updated note 1 in Table 3–9. ● Updated note 1 in Figure 3–40. ● Updated note 2 in Figure 3–41. ● Updated Table 3–16. ● Updated Figure 3–56. ● Updated Tables 3–19 through 3–22. ● Updated Tables 3–25 and 3–26. ● Updated “Fast PLL & Channel Layout” section. | Added 1,152-pin FineLine BGA package information for EP2SGX60 device in Table 3–16. |

| Table 2–42. Document Revision History (Part 6 of 6) | | |
|--|---|---------------------------|
| Date and Document Version | Changes Made | Summary of Changes |
| <i>Previous Chapter 03 changes:</i> December 2005 v1.1 | Updated Figure 3–56. | |
| <i>Previous Chapter 03 changes:</i> October 2005 v1.0 | Added chapter to the <i>Stratix II GX Device Handbook</i> . | |

IEEE Std. 1149.1 JTAG Boundary- Scan Support

All Stratix® II GX devices provide Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry that complies with the IEEE Std. 1149.1. You can perform JTAG boundary-scan testing either before or after, but not during configuration. Stratix II GX devices can also use the JTAG port for configuration with the Quartus® II software or hardware using either Jam Files (.jam) or Jam Byte-Code Files (.jbc).

Stratix II GX devices support IOE I/O standard setting reconfiguration through the JTAG BST chain. The JTAG chain can update the I/O standard for all input and output pins any time before or during user mode through the CONFIG_IO instruction. You can use this capability for JTAG testing before configuration when some of the Stratix II GX pins drive or receive from other devices on the board using voltage-referenced standards. Since the Stratix II GX device may not be configured before JTAG testing, the I/O pins may not be configured for appropriate electrical standards for chip-to-chip communication. Programming these I/O standards via JTAG allows you to fully test I/O connections to other devices.

A device operating in JTAG mode uses four required pins, TDI, TDO, TMS, and TCK, and one optional pin, TRST. The TCK pin has an internal weak pull-down resistor, while the TDI, TMS, and TRST pins have weak internal pull-up resistors. The JTAG input pins are powered by the 3.3-V VCCPD pins. The TDO output pin is powered by the VCCIO power supply in I/O bank 4.

Stratix II GX devices also use the JTAG port to monitor the logic operation of the device with the SignalTap® II embedded logic analyzer. Stratix II GX devices support the JTAG instructions shown in [Table 3-1](#).



Stratix II GX devices must be within the first eight devices in a JTAG chain. All of these devices have the same JTAG controller. If any of the Stratix II GX devices appear after the eighth device in the JTAG chain, they will fail configuration. This does not affect SignalTap II embedded logic analysis.

Table 3–1. Stratix II GX JTAG Instructions

| JTAG Instruction | Instruction Code | Description |
|---------------------------|------------------|--|
| SAMPLE/PRELOAD | 00 0000 0101 | Allows a snapshot of signals at the device pins to be captured and examined during normal device operation and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer. |
| EXTEST(1) | 00 0000 1111 | Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins. |
| BYPASS | 11 1111 1111 | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation. |
| USERCODE | 00 0000 0111 | Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO. |
| IDCODE | 00 0000 0110 | Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO. |
| HIGHZ (1) | 00 0000 1011 | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins. |
| CLAMP (1) | 00 0000 1010 | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding the I/O pins to a state defined by the data in the boundary-scan register. |
| ICR instructions | | Used when configuring a Stratix II GX device via the JTAG port with a USB-Blaster™, MasterBlaster™, ByteBlasterMV™, or ByteBlaster II download cable, or when using a .jam or .jbc via an embedded processor or JRunner. |
| PULSE_NCONFIG | 00 0000 0001 | Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected. |
| CONFIG_IO (2) | 00 0000 1101 | Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, during, or after configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction holds nSTATUS low to reset the configuration device. nSTATUS is held low until the IOE configuration register is loaded and the TAP controller state machine transitions to the UPDATE_DR state. |
| SignalTap II instructions | | Monitors internal device operation with the SignalTap II embedded logic analyzer. |

Notes to Table 3–1:

- (1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.
- (2) For more information on using the CONFIG_IO instruction, refer to the *MorphIO: An I/O Reconfiguration Solution for Altera Devices White Paper*.

The Stratix II GX device instruction register length is 10 bits and the USERCODE register length is 32 bits. Tables 3–2 and 3–3 show the boundary-scan register length and device IDCODE information for Stratix II GX devices.

Table 3–2. Stratix II GX Boundary-Scan Register Length

| Device | Boundary-Scan Register Length |
|-----------|-------------------------------|
| EP2SGX30 | 1,320 |
| EP2SGX60 | 1,506 |
| EP2SGX90 | 2,016 |
| EP2SGX130 | 2,454 |

Table 3–3. 32-Bit Stratix II GX Device IDCODE

| Device | IDCODE (32 Bits) | | | |
|-----------|------------------|-----------------------|---------------------------------|-------------|
| | Version (4 Bits) | Part Number (16 Bits) | Manufacturer Identity (11 Bits) | LSB (1 Bit) |
| EP2SGX30 | 0000 | 0010 0000 1110 0001 | 000 0110 1110 | 1 |
| EP2SGX60 | 0000 | 0010 0000 1110 0010 | 000 0110 1110 | 1 |
| EP2SGX90 | 0000 | 0010 0000 1110 0011 | 000 0110 1110 | 1 |
| EP2SGX130 | 0000 | 0010 0000 1110 0100 | 000 0110 1110 | 1 |

SignalTap II Embedded Logic Analyzer

Stratix II GX devices feature the SignalTap II embedded logic analyzer, which monitors design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry. You can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages, such as FineLine BGA packages, because it can be difficult to add a connection to a pin during the debugging process after a board is designed and manufactured.

Configuration

The logic, circuitry, and interconnects in the Stratix II GX architecture are configured with CMOS SRAM elements. Altera® FPGAs are reconfigurable and every device is tested with a high coverage production test program so you do not have to perform fault testing and can instead focus on simulation and design verification.

Stratix II GX devices are configured at system power-up with data stored in an Altera configuration device or provided by an external controller (for example, a MAX® II device or microprocessor). You can configure Stratix II GX devices using the fast passive parallel (FPP), active serial

(AS), passive serial (PS), passive parallel asynchronous (PPA), and JTAG configuration schemes. The Stratix II GX device's optimized interface allows microprocessors to configure it serially or in parallel and synchronously or asynchronously. The interface also enables microprocessors to treat Stratix II GX devices as memory and configure them by writing to a virtual memory location, making reconfiguration easy.

In addition to the number of configuration methods supported, Stratix II GX devices also offer the design security, decompression, and remote system upgrade features. The design security feature, using configuration bitstream encryption and advanced encryption standard (AES) technology, provides a mechanism to protect designs. The decompression feature allows Stratix II GX FPGAs to receive a compressed configuration bitstream and decompress this data in real-time, reducing storage requirements and configuration time. The remote system upgrade feature allows real-time system upgrades from remote locations of Stratix II GX designs. For more information, refer to the ["Configuration Schemes" on page 3–6](#).

Operating Modes

The Stratix II GX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

SRAM configuration elements allow you to reconfigure Stratix II GX devices in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, re-initializes the device, and resumes user-mode operation. You can perform in-field upgrades by distributing new configuration files either within the system or remotely.

The `PORSEL` pin is a dedicated input used to select power-on reset (POR) delay times of 12 ms or 100 ms during power up. When the `PORSEL` pin is connected to ground, the POR time is 100 ms. When the `PORSEL` pin is connected to V_{CC} , the POR time is 12 ms.

The `nIO_PULLUP` pin is a dedicated input that chooses whether the internal pull-up resistors on the user I/O pins and dual-purpose configuration I/O pins (`nCSO`, `ASDO`, `DATA [7..0]`, `nWS`, `nRS`, `RDYnBSY`, `nCS`, `CS`, `RUnLU`, `PGM [2..0]`, `CLKUSR`, `INIT_DONE`, `DEV_OE`, `DEV_CLR`) are on or off before and during configuration. A logic high (1.5, 1.8, 2.5, 3.3 V) turns off the weak internal pull-up resistors, while a logic low turns them on.

Stratix II GX devices also offer a new power supply, V_{CCPD} , which must be connected to 3.3 V in order to power the 3.3-V/2.5-V buffer available on the configuration input pins and JTAG pins. V_{CCPD} applies to all the JTAG input pins (`TCK`, `TMS`, `TDI`, and `TRST`) and the following configuration pins: `nCONFIG`, `DCLK` (when used as an input), `nIO_PULLUP`, `DATA [7..0]`, `RUnLU`, `nCE`, `nWS`, `nRS`, `CS`, `nCS`, and `CLKUSR`. The `VCCSEL` pin allows the V_{CCIO} setting (of the banks where the configuration inputs reside) to be independent of the voltage required by the configuration inputs. Therefore, when selecting the V_{CCIO} voltage, you do not have to take the V_{IL} and V_{IH} levels driven to the configuration inputs into consideration. The configuration input pins, `nCONFIG`, `DCLK` (when used as an input), `nIO_PULLUP`, `RUnLU`, `nCE`, `nWS`, `nRS`, `CS`, `nCS`, and `CLKUSR`, have a dual buffer design: a 3.3-V/2.5-V input buffer and a 1.8-V/1.5-V input buffer. The `VCCSEL` input pin selects which input buffer is used. The 3.3-V/2.5-V input buffer is powered by V_{CCPD} , while the 1.8-V/1.5-V input buffer is powered by V_{CCIO} .

V_{CCSEL} is sampled during power-up. Therefore, the `VCCSEL` setting cannot change on-the-fly or during a reconfiguration. The `VCCSEL` input buffer is powered by V_{CCINT} and must be hardwired to V_{CCPD} or ground. A logic high `VCCSEL` connection selects the 1.8-V/1.5-V input buffer; a logic low selects the 3.3-V/2.5-V input buffer. `VCCSEL` should be set to comply with the logic levels driven out of the configuration device or the MAX II microprocessor.

If the design must support configuration input voltages of 3.3 V/2.5 V, set `VCCSEL` to a logic low. You can set the V_{CCIO} voltage of the I/O bank that contains the configuration inputs to any supported voltage. If the design must support configuration input voltages of 1.8 V/1.5 V, set `VCCSEL` to a logic high and the V_{CCIO} of the bank that contains the configuration inputs to 1.8 V/1.5 V.



For more information on multi-volt support, including information on using `TDO` and `nCEO` in multi-volt systems, refer to the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Configuration Schemes

You can load the configuration data for a Stratix II GX device with one of five configuration schemes (refer to [Table 3–4](#)), chosen on the basis of the target application. You can use a configuration device, intelligent controller, or the JTAG port to configure a Stratix II GX device. A configuration device can automatically configure a Stratix II GX device at system power-up.

Multiple Stratix II GX devices can be configured in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device. Stratix II GX FPGAs offer the following:

- Configuration data decompression to reduce configuration file storage
- Design security using configuration data encryption to protect designs
- Remote system upgrades for remotely updating Stratix II GX designs

[Table 3–4](#) summarizes which configuration features can be used in each configuration scheme.



Refer to the [Configuring Stratix II & Stratix II GX Devices](#) chapter in volume 2 of the *Stratix II GX Device Handbook* for more information about configuration schemes in Stratix II GX devices.

| Configuration Scheme | Configuration Method | Design Security | Decompression | Remote System Upgrade |
|----------------------|--|-----------------|---------------|-----------------------|
| FPP | MAX II device or microprocessor and flash device | ✓ (1) | ✓ (1) | ✓ |
| | Enhanced configuration device | | ✓ (2) | ✓ |
| AS | Serial configuration device | ✓ | ✓ | ✓ (3) |
| PS | MAX II device or microprocessor and flash device | ✓ | ✓ | ✓ |
| | Enhanced configuration device | ✓ | ✓ | ✓ |
| | Download cable (4) | ✓ | ✓ | |
| PPA | MAX II device or microprocessor and flash device | | | ✓ |

Table 3–4. Stratix II GX Configuration Features (Part 2 of 2)

| Configuration Scheme | Configuration Method | Design Security | Decompression | Remote System Upgrade |
|----------------------|--|-----------------|---------------|-----------------------|
| JTAG | Download cable (4) | | | |
| | MAX II device or microprocessor and flash device | | | |

Notes for Table 3–4:

- (1) In these modes, the host system must send a DCLK that is 4× the data rate.
- (2) The enhanced configuration device decompression feature is available, while the Stratix II GX decompression feature is not available.
- (3) Only remote update mode is supported when using the AS configuration scheme. Local update mode is not supported.
- (4) The supported download cables include the Altera USB-Blaster universal serial bus (USB) port download cable, MasterBlaster serial/USB communications cable, ByteBlaster II parallel port download cable, and the ByteBlasterMV parallel port download cable.

Device Security Using Configuration Bitstream Encryption

Stratix II and Stratix II GX FPGAs are the industry’s first FPGAs with the ability to decrypt a configuration bitstream using the AES algorithm. When using the design security feature, a 128-bit security key is stored in the Stratix II GX FPGA. To successfully configure a Stratix II GX FPGA that has the design security feature enabled, the device must be configured with a configuration file that was encrypted using the same 128-bit security key. The security key can be stored in non-volatile memory inside the Stratix II GX device. This nonvolatile memory does not require any external devices, such as a battery back up, for storage.



An encrypted configuration file is the same size as a non-encrypted configuration file. When using a serial configuration scheme such as passive serial (PS) or active serial (AS), configuration time is the same whether or not the design security feature is enabled. If the fast passive parallel (FPP) scheme is used with the design security or decompression feature, a 4× DCLK is required. This results in a slower configuration time when compared to the configuration time of an FPGA that has neither the design security nor the decompression feature enabled. For more information about this feature, contact an Altera sales representative.

Device Configuration Data Decompression

Stratix II GX FPGAs support decompression of configuration data, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other

memory, and transmit this compressed bitstream to Stratix II GX FPGAs. During configuration, the Stratix II GX FPGA decompresses the bitstream in real time and programs its SRAM cells. Stratix II GX FPGAs support decompression in the FPP (when using a MAX II device or microprocessor and flash memory), AS, and PS configuration schemes. Decompression is not supported in the PPA configuration scheme nor in JTAG-based configuration.

Remote System Upgrades

Shortened design cycles, evolving standards, and system deployments in remote locations are difficult challenges faced by system designers. Stratix II GX devices can help effectively deal with these challenges with their inherent reprogrammability and dedicated circuitry to perform remote system updates. Remote system updates help deliver feature enhancements and bug fixes without costly recalls, reducing time to market, and extending product life.

Stratix II GX FPGAs feature dedicated remote system upgrade circuitry to facilitate remote system updates. Soft logic (Nios processor or user logic) implemented in the Stratix II GX device can download a new configuration image from a remote location, store it in configuration memory, and direct the dedicated remote system upgrade circuitry to initiate a reconfiguration cycle. The dedicated circuitry performs error detection during and after the configuration process, recovers from any error condition by reverting back to a safe configuration image, and provides error status information. This dedicated remote system upgrade circuitry avoids system downtime and is the critical component for successful remote system upgrades.

Remote system configuration is supported in the following Stratix II GX configuration schemes: FPP, AS, PS, and PPA. Remote system configuration can also be implemented in conjunction with Stratix II GX features such as real-time decompression of configuration data and design security using AES for secure and efficient field upgrades.



Refer to the *Remote System Upgrades with Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook* for more information about remote configuration in Stratix II GX devices.

Configuring Stratix II GX FPGAs with JRunner

The JRunner™ software driver configures Altera FPGAs, including Stratix II GX FPGAs, through the ByteBlaster II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in Raw Binary File (.rbf) format. JRunner also requires a Chain Description File (.cdf)

generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code is developed for the Windows NT operating system (OS), but can be customized to run on other platforms.



For more information on the JRunner software driver, refer to the *AN 414: An Embedded Solution for PLD JTAG Configuration* and the source files on the Altera web site (www.altera.com).

Programming Serial Configuration Devices with SRrunner

A serial configuration device can be programmed in-system by an external microprocessor using SRrunner. SRrunner is a software driver developed for embedded serial configuration device programming that can be easily customized to fit into different embedded systems. SRrunner reads a Raw Programming Data file (.rpd) and writes to serial configuration devices. The serial configuration device programming time using SRrunner is comparable to the programming time when using the Quartus II software.



For more information about SRrunner, refer to the *AN 418 SRrunner: An Embedded Solution for Serial Configuration Device Programming* and the source code on the Altera web site.



For more information on programming serial configuration devices, refer to the *Serial Configuration Devices (EPCS1, EPCS4, EPCS64, and EPCS128) Data Sheet* in the *Configuration Handbook*.

Configuring Stratix II FPGAs with the MicroBlaster Driver

The MicroBlaster software driver supports an RBF programming input file and is ideal for embedded FPP or PS configuration. The source code is developed for the Windows NT operating system, although it can be customized to run on other operating systems.



For more information on the MicroBlaster software driver, refer to the *Configuring the MicroBlaster Fast Passive Parallel Software Driver White Paper* or the *Configuring the MicroBlaster Passive Serial Software Driver White Paper* on the Altera web site.

PLL Reconfiguration

The phase-locked loops (PLLs) in the Stratix II GX device family support reconfiguration of their multiply, divide, VCO-phase selection, and bandwidth selection settings without reconfiguring the entire device. You can use either serial data from the logic array or regular I/O pins to program the PLL's counter settings in a serial chain. This option provides

considerable flexibility for frequency synthesis, allowing real-time variation of the PLL frequency and delay. The rest of the device is functional while reconfiguring the PLL.



See the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook* for more information on Stratix II GX PLLs.

Temperature Sensing Diode (TSD)

Stratix II GX devices include a diode-connected transistor for use as a temperature sensor in power management. This diode is used with an external digital thermometer device. These devices steer bias current through the Stratix II GX diode, measuring forward voltage and converting this reading to temperature in the form of an 8-bit signed number (7 bits plus 1 sign bit). The external device's output represents the junction temperature of the Stratix II GX device and can be used for intelligent power management.

The diode requires two pins (`tempdiodep` and `tempdioden`) on the Stratix II GX device to connect to the external temperature-sensing device, as shown in [Figure 3-1](#). The temperature sensing diode is a passive element and therefore can be used before the Stratix II GX device is powered.

Figure 3-1. External Temperature-Sensing Diode

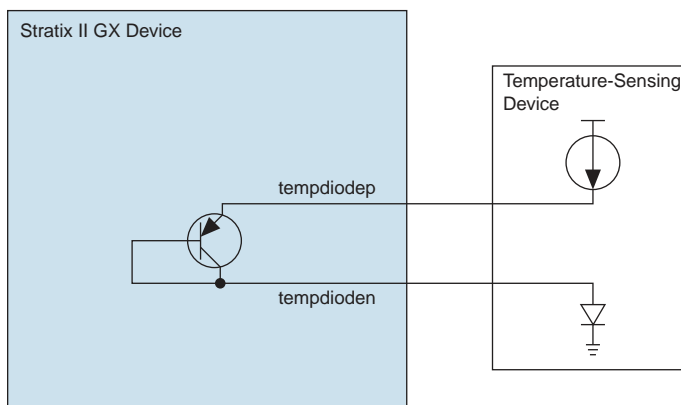
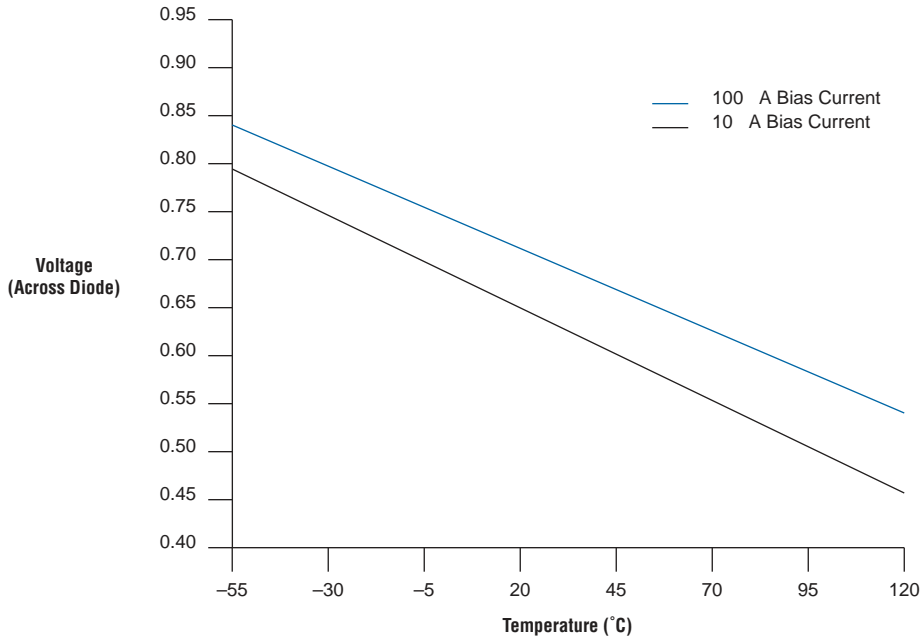


Table 3-5 shows the specifications for bias voltage and current of the Stratix II GX temperature sensing diode.

| Parameter | Minimum | Typical | Maximum | Unit |
|-------------------|---------|---------|---------|---------------|
| IBIAS high | 80 | 100 | 120 | μA |
| IBIAS low | 8 | 10 | 12 | μA |
| VBP - VBN | 0.3 | | 0.9 | V |
| VBN | | 0.7 | | V |
| Series resistance | | | 3 | Ω |

The temperature-sensing diode works for the entire operating range shown in Figure 3-2.

Figure 3-2. Temperature Versus Temperature-Sensing Diode Voltage



The temperature sensing diode is a very sensitive circuit which can be influenced by noise coupled from other traces on the board, and possibly within the device package itself, depending on device usage. The interfacing device registers temperature based on millivolts of difference as seen at the TSD. Switching I/O near the TSD pins can affect the temperature reading. Altera recommends you take temperature readings during periods of no activity in the device (for example, standby mode where no clocks are toggling in the device), such as when the nearby I/Os are at a DC state, and disable clock networks in the device.

Automated Single Event Upset (SEU) Detection

Stratix II GX devices offer on-chip circuitry for automated checking of single event upset (SEU) detection. Some applications that require the device to operate error free at high elevations or in close proximity to Earth's North or South Pole will require periodic checks to ensure continued data integrity. The error detection cyclic redundancy check (CRC) feature controlled by the **Device & Pin Options** dialog box in the Quartus II software uses a 32-bit CRC circuit to ensure data reliability and is one of the best options for mitigating SEU.

You can implement the error detection CRC feature with existing circuitry in Stratix II GX devices, eliminating the need for external logic. Stratix II GX devices compute CRC during configuration and checks the computed-CRC against an automatically computed CRC during normal operation. The `CRC_ERROR` pin reports a soft error when configuration SRAM data is corrupted, triggering device reconfiguration.

Custom-Built Circuitry

Dedicated circuitry is built into Stratix II GX devices to automatically perform error detection. This circuitry constantly checks for errors in the configuration SRAM cells while the device is in user mode. You can monitor one external pin for the error and use it to trigger a reconfiguration cycle. You can select the desired time between checks by adjusting a built-in clock divider.

Software Interface

Beginning with version 4.1 of the Quartus II software, you can turn on the automated error detection CRC feature in the **Device & Pin Options** dialog box. This dialog box allows you to enable the feature and set the internal frequency of the CRC between 400 kHz to 50 MHz. This controls the rate that the CRC circuitry verifies the internal configuration SRAM bits in the Stratix II GX FPGA.



For more information on CRC, refer to [AN 357: Error Detection Using CRC in Altera FPGA Devices](#).

Referenced Documents

This chapter references the following documents:

- *AN 357: Error Detection Using CRC in Altera FPGA Devices*
- *AN 414: An Embedded Solution for PLD JTAG Configuration*
- *AN 418 SRrunner: An Embedded Solution for Serial Configuration Device Programming*
- *Configuring Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*
- *Configuring the MicroBlaster Fast Passive Parallel Software Driver White Paper*
- *Configuring the MicroBlaster Passive Serial Software Driver White Paper*
- *MorphIO: An I/O Reconfiguration Solution for Altera Devices White Paper*
- *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*
- *Remote System Upgrades with Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*
- *Serial Configuration Devices (EPCS1, EPCS4, EPCS64, and EPCS128) Data Sheet* in the *Configuration Handbook*
- *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Document Revision History

Table 3–6 shows the revision history for this chapter.

| Date and Document Version | Changes Made | Summary of Changes |
|----------------------------------|---|---|
| October 2007 v1.4 | Minor text edits. | — |
| August 2007 v1.3 | Updated the note in the “ IEEE Std. 1149.1 JTAG Boundary-Scan Support ” | — |
| | Updated Table 3–3 . | — |
| | Added the “ Referenced Documents ” section. | — |
| May 2007 v1.2 | Updated the “Temperature Sensing Diode (TSD)” section. | — |
| February 2007 v1.1 | Added the “Document Revision History” section to this chapter. | Added support information for the Stratix II GX device. |
| October 2005 v1.0 | Added chapter to the <i>Stratix II GX Device Handbook</i> . | — |

Operating Conditions

Stratix® II GX devices are offered in both commercial and industrial grades. Industrial devices are offered in -4 speed grade and commercial devices are offered in -3 (fastest), -4, and -5 speed grades.

Tables 4-1 through 4-51 provide information on absolute maximum ratings, recommended operating conditions, DC electrical characteristics, and other specifications for Stratix II GX devices.

Absolute Maximum Ratings

Table 4-1 contains the absolute maximum ratings for the Stratix II GX device family.

Table 4-1. Stratix II GX Device Absolute Maximum Ratings *Notes (1), (2),(3)*

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|--------------------|----------------------------|-------------------------|---------|---------|------|
| V _{CCINT} | Supply voltage | With respect to ground | -0.5 | 1.8 | V |
| V _{CCIO} | Supply voltage | With respect to ground | -0.5 | 4.6 | V |
| V _{CCPD} | Supply voltage | With respect to ground | -0.5 | 4.6 | V |
| V _I | DC input voltage (4) | | -0.5 | 4.6 | V |
| I _{OUT} | DC output current, per pin | | -25 | 40 | mA |
| T _{STG} | Storage temperature | No bias | -65 | 150 | C |
| T _J | Junction temperature | BGA packages under bias | -55 | 125 | C |

Notes to Table 4-1:

- (1) See the *Operating Requirements for Altera Devices Data Sheet* for more information.
- (2) Conditions beyond those listed in Table 4-1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.
- (3) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.
- (4) During transitions, the inputs may overshoot to the voltage shown in Table 4-2 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transitions, the inputs may undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 4–2. Maximum Duty Cycles in Voltage Transitions

| Symbol | Parameter | Condition | Maximum Duty Cycles (%) (1) |
|----------------|--|------------------------|-----------------------------|
| V _I | Maximum duty cycles in voltage transitions | V _I = 4.0 V | 100 |
| | | V _I = 4.1 V | 90 |
| | | V _I = 4.2 V | 50 |
| | | V _I = 4.3 V | 30 |
| | | V _I = 4.4 V | 17 |
| | | V _I = 4.5 V | 10 |

Note to Table 4–2:

- (1) During transition, the inputs may overshoot to the voltages shown based on the input duty cycle. The duty cycle case is equivalent to 100% duty cycle.

Recommended Operating Conditions

Table 4–3 contains the Stratix II GX device family recommended operating conditions.

Table 4–3. Stratix II GX Device Recommended Operating Conditions (Part 1 of 2) Note (1)

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|--------------------|---|--------------------------------------|-----------------|-------------------|------|
| V _{CCINT} | Supply voltage for internal logic and input buffers | 100 μs ≤ rise time ≤ 100 ms (3) | 1.15 | 1.25 | V |
| V _{CCIO} | Supply voltage for output buffers, 3.3-V operation | 100 μs ≤ rise time ≤ 100 ms (3), (6) | 3.135 (3.00) | 3.465 (3.60) | V |
| | Supply voltage for output buffers, 2.5-V operation | 100 μs ≤ rise time ≤ 100 ms (3) | 2.375 | 2.625 | V |
| | Supply voltage for output buffers, 1.8-V operation | 100 μs ≤ rise time ≤ 100 ms (3) | 1.71 | 1.89 | V |
| | Supply voltage for output buffers, 1.5-V operation | 100 μs ≤ rise time ≤ 100 ms (3) | 1.425 | 1.575 | V |
| | Supply voltage for output buffers, 1.2-V operation | 100 μs ≤ rise time ≤ 100 ms (3) | 1.15 | 1.25 | V |
| V _{CCPD} | Supply voltage for pre-drivers as well as configuration and JTAG I/O buffers. | 100 μs ≤ rise time ≤ 100 ms (4) | 3.135 | 3.465 | V |
| V _I | Input voltage (see Table 4–2) | (2), (5) | –0.5 | 4.0 | V |
| V _O | Output voltage | | 0 | V _{CCIO} | V |

Table 4–3. Stratix II GX Device Recommended Operating Conditions (Part 2 of 2) *Note (1)*

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|----------------|--------------------------------|--------------------|---------|---------|------|
| T _J | Operating junction temperature | For commercial use | 0 | 85 | C |
| | | For industrial use | –40 | 100 | C |

Notes to Table 4–3:

- (1) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.
- (2) During transitions, the inputs may overshoot to the voltage shown in Table 4–2 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically from ground to V_{CC}.
- (4) V_{CCPD} must ramp-up from 0 V to 3.3 V within 100 μs to 100 ms. If V_{CCPD} is not ramped up within this specified time, the Stratix II GX device will not configure successfully. If the system does not allow for a V_{CCPD} ramp-up time of 100 ms or less, hold nCONFIG low until all power supplies are reliable.
- (5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT}, V_{CCPD}, and V_{CCIO} are powered.
- (6) V_{CCIO} maximum and minimum conditions for PCI and PCI-X are shown in parentheses.

Transceiver Block Characteristics

Tables 4–4 through 4–6 contain transceiver block specifications.

Table 4–4. Stratix II GX Transceiver Block Absolute Maximum Ratings *Note (1)*

| Symbol | Parameter | Conditions | Minimum | Maximum | Units |
|--------------------|----------------------------------|---------------------------|---------|---------|-------|
| V _{CCA} | Transceiver block supply voltage | Commercial and industrial | –0.5 | 4.6 | V |
| V _{CCP} | Transceiver block supply voltage | Commercial and industrial | –0.5 | 1.8 | V |
| V _{CCR} | Transceiver block supply Voltage | Commercial and industrial | –0.5 | 1.8 | V |
| V _{CCT} | Transceiver block supply voltage | Commercial and industrial | –0.5 | 1.8 | V |
| V _{CCT_B} | Transceiver block supply voltage | Commercial and industrial | –0.5 | 1.8 | V |
| V _{CCL} | Transceiver block supply voltage | Commercial and industrial | –0.5 | 1.8 | V |
| V _{CCH_B} | Transceiver block supply voltage | Commercial and industrial | –0.5 | 2.4 | V |

Note to Table 4–4:

- (1) The device can tolerate prolonged operation at this absolute maximum, as long as the maximum specification is not violated.

Table 4–5. Stratix II GX Transceiver Block Operating Conditions

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|------------------------|----------------------------------|---------------------------|----------|---------|----------|-------|
| V _{CCA} | Transceiver block supply voltage | Commercial and industrial | 3.135 | 3.3 | 3.465 | V |
| V _{CCP} | Transceiver block supply voltage | Commercial and industrial | 1.15 | 1.2 | 1.25 | V |
| V _{CCR} | Transceiver block supply voltage | Commercial and industrial | 1.15 | 1.2 | 1.25 | V |
| V _{CCT} | Transceiver block supply voltage | Commercial and industrial | 1.15 | 1.2 | 1.25 | V |
| V _{CCT_B} | Transceiver block supply voltage | Commercial and industrial | 1.15 | 1.2 | 1.25 | V |
| V _{CCL} | Transceiver block supply voltage | Commercial and industrial | 1.15 | 1.2 | 1.25 | V |
| V _{CCH_B} (2) | Transceiver block supply voltage | Commercial and industrial | 1.15 | 1.2 | 1.25 | V |
| | | | 1.425 | 1.5 | 1.575 | V |
| R _{REF} (1) | Reference resistor | Commercial and industrial | 2000 –1% | 2000 | 2000 +1% | Ω |

Notes to Table 4–5:

- (1) The DC signal on this pin must be as clean as possible. Ensure that no noise is coupled to this pin.
- (2) Refer to the *Stratix II GX Device Handbook, volume 2*, for more information.

Table 4–6. Stratix II GX Transceiver Block AC Specification (Part 1 of 6)

| Symbol / Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|---|------------|---|-----|--------|--|-----|--------|---------------------------------|-----|--------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Reference clock | | | | | | | | | | | |
| Input frequency from REFCLK input | | 50 | - | 622.08 | 50 | - | 622.08 | 50 | - | 622.08 | MHz |
| Input frequency from PLD input | | 50 | - | 325 | 50 | - | 325 | 50 | - | 325 | MHz |
| Input clock jitter | | Refer to Table 4–20 on page 4–36 for the input jitter specifications for the reference clock. | | | | | | | | | |
| Absolute V _{MAX} for a REFCLK pin (12) | | - | - | 3.3 | - | - | 3.3 | - | - | 3.3 | V |

Table 4–6. Stratix II GX Transceiver Block AC Specification (Part 2 of 6)

| Symbol / Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|--|-----------------------------|---------------------------------|-----|---------------------|--|-----|---------------------|---------------------------------|-----|---------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Absolute V_{MIN} for a REFCLK pin (12) | | -0.3 | - | - | -0.3 | - | - | -0.3 | - | - | V |
| Rise/fall time | | - | 0.2 | - | - | 0.2 | - | - | 0.2 | - | UI |
| Duty cycle | | 40 | - | 60 | 40 | - | 60 | 40 | - | 60 | % |
| Peak-to-peak differential input voltage | | 200 | - | 2000 | 200 | - | 2000 | 200 | - | 2000 | mV |
| Spread-spectrum clocking | | 30 0 to -0.5% | - | 33 0 to -0.5% | 30 0 to -0.5% | - | 33 0 to -0.5% | 30 0 to -0.5% | - | 33 0 to -0.5% | kHz |
| On-chip termination resistors | | 115 ±20% | | | 115 ±20% | | | 115 ±20% | | | Ω |
| V_{ICM} (AC coupled) (12) | | 1200 ±5% | | | 1200 ±5% | | | 1200 ±5% | | | mV |
| V_{ICM} (DC coupled) (4) | | 0.25 | - | 0.55 | 0.25 | - | 0.55 | 0.25 | - | 0.55 | V |
| Rref | | 2000 ±1% | | | 2000 ±1% | | | 2000 ±1% | | | Ω |
| Transceiver Clocks | | | | | | | | | | | |
| Calibration block clock frequency | | 10 | - | 125 | 10 | - | 125 | 10 | - | 125 | MHz |
| Calibration block minimum power-down pulse width | | 30 | - | - | 30 | - | - | 30 | - | - | ns |
| Time taken for one-time calibration | | - | - | 8 | - | - | 8 | - | - | 8 | ms |
| fixedclk clock frequency | PCI Express Receiver Detect | - | 125 | - | - | 125 | - | - | 125 | - | MHz |
| | Adaptive Equalization (AEQ) | 2.5 | - | 125 | 2.5 | - | 125 | - | - | - | MHz |

Table 4–6. Stratix II GX Transceiver Block AC Specification (Part 3 of 6)

| Symbol / Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|---|--|---------------------------------|-----|------|--|-----|------|---------------------------------|-----|------|----------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| reconfig_clk clock frequency | | 2.5 | - | 50 | 2.5 | - | 50 | 2.5 | - | 50 | MHz |
| Transceiver block minimum power-down pulse width | | 100 | - | - | 100 | - | - | 100 | - | - | ns |
| Receiver | | | | | | | | | | | |
| Data rate | | 600 | - | 6375 | 600 | - | 5000 | 600 | - | 4250 | Mbps |
| Absolute V_{MAX} for a receiver pin (1) | | - | - | 2.0 | - | - | 2.0 | - | - | 2.0 | V |
| Absolute V_{MIN} for a receiver pin | | -0.4 | - | - | -0.4 | - | - | -0.4 | - | - | V |
| Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) | $V_{CM} = 0.85$ V | - | - | 3.3 | - | - | 3.3 | - | - | 3.3 | V |
| Minimum peak-to-peak differential input voltage V_{ID} (diff p-p) | $V_{CM} = 0.85$ V DC Gain = ≥ 3 dB | 160 | - | - | 160 | - | - | 160 | - | - | mV |
| V_{ICM} | $V_{ICM} = 0.85$ V setting | 850 \pm 10% | | | 850 \pm 10% | | | 850 \pm 10% | | | mV |
| | $V_{ICM} = 1.2$ V setting (11) | 1200 \pm 10% | | | 1200 \pm 10% | | | 1200 \pm 10% | | | mV |
| On-chip termination resistors | 100 Ω setting | 100 \pm 15% | | | 100 \pm 15% | | | 100 \pm 15% | | | Ω |
| | 120 Ω setting | 120 \pm 15% | | | 120 \pm 15% | | | 120 \pm 15% | | | Ω |
| | 150 Ω setting | 150 \pm 15% | | | 150 \pm 15% | | | 150 \pm 15% | | | Ω |
| Bandwidth at 6.375 Gbps | BW = Low | - | 20 | - | - | - | - | - | - | - | MHz |
| | BW = Med | - | 35 | - | - | - | - | - | - | - | MHz |
| | BW = High | - | 45 | - | - | - | - | - | - | - | MHz |

Table 4–6. Stratix II GX Transceiver Block AC Specification (Part 4 of 6)

| Symbol / Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|--|------------|--|-----|------|--|-----|------|---|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Bandwidth at 3.125 Gbps | BW = Low | - | 30 | - | - | 30 | - | - | 30 | - | MHz |
| | BW = Med | - | 40 | - | - | 40 | - | - | 40 | - | MHz |
| | BW = High | - | 50 | - | - | 50 | - | - | 50 | - | MHz |
| Bandwidth at 2.5 Gbps | BW = Low | - | 35 | - | - | 35 | - | - | 35 | - | MHz |
| | BW = Med | - | 50 | - | - | 50 | - | - | 50 | - | MHz |
| | BW = High | - | 60 | - | - | 60 | - | - | 60 | - | MHz |
| Return loss differential mode | | 100 MHz to 2.5 GHz (XAUI): -10 dB 50 MHz to 1.25 GHz (PCI-E): -10 dB 100 MHz to 4.875 GHz (OIF/CEI): -8dB 4.875 GHz to 10 GHz (OIF/CEI): 16.6 dB/decade slope | | | | | | | | | |
| Return loss common mode | | 100 MHz to 2.5 GHz (XAUI): -6 dB 50 MHz to 1.25 GHz (PCI-E): -6 dB 100 MHz to 4.875 GHz (OIF/CEI): -6dB 4.875 GHz to 10 GHz (OIF/CEI): 16.6 dB/decade slope | | | | | | | | | |
| Programmable PPM detector (2) | | ±62.5, 100, 125, 200, 250, 300, 500, 1000 | | | ±62.5, 100, 125, 200, 250, 300, 500, 1000 | | | ±62.5, 100, 125, 200, 250, 300, 500, 1000 | | | ppm |
| Run length (3), (9) | | 80 | | | 80 | | | 80 | | | UI |
| Programmable equalization | | - | - | 16 | - | - | 16 | - | - | 16 | dB |
| Signal detect/loss threshold (4) | | 65 | - | 175 | 65 | - | 175 | 65 | - | 175 | mV |
| CDR LTR Time (5), (9) | | - | - | 75 | - | - | 75 | - | - | 75 | us |
| CDR Minimum T1b (6), (9) | | 15 | - | - | 15 | - | - | 15 | - | - | us |
| LTD lock time (7), (9) | | 0 | 100 | 4000 | 0 | 100 | 4000 | 0 | 100 | 4000 | ns |
| Data lock time from rx_freqlocked (8), (9) | | - | - | 4 | - | - | 4 | - | - | 4 | us |
| Programmable DC gain | | 0, 3, 6 | | | 0, 3, 6 | | | 0, 3, 6 | | | dB |
| Transmitter | | | | | | | | | | | |

Table 4–6. Stratix II GX Transceiver Block AC Specification (Part 5 of 6)

| Symbol / Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|-----------------------------------|---|---------------------------------|-----|--------|--|-----|--------|---------------------------------|-----|--------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Data rate | | 600 | - | 6375 | 600 | - | 5000 | 600 | - | 4250 | Mbps |
| V_{OCM} | $V_{OCM} = 0.6$ V setting | 580±10% | | | 580±10% | | | 580±10% | | | mV |
| | $V_{OCM} = 0.7$ V setting | 680±10% | | | 680±10% | | | 680±10% | | | mV |
| On-chip termination resistors | 100 Ω setting | 108±10% | | | 108±10% | | | 108±10% | | | Ω |
| | 120 Ω setting | 125±10% | | | 125±10% | | | 125±10% | | | Ω |
| | 150 Ω setting | 152±10% | | | 152±10% | | | 152±10% | | | Ω |
| Return loss differential mode | 312 MHz to 625 MHz (XAUI): -10 dB 625 MHz to 3.125 GHz (XAUI): -10 dB/decade slope 50 MHz to 1.25 GHz (PCI-E): -10dB 100 MHz to 4.875 GHz (OIF/CEI): -8db 4.875 GHz to 10 GHz (OIF/CEI): 16.6 dB/decade slope | | | | | | | | | | |
| Return loss common mode | 50 MHz to 1.25 GHz (PCI-E): -6dB 100 MHz to 4.875 GHz (OIF/CEI): -6db 4.875 GHz to 10 GHz (OIF/CEI): 16.6 dB/decade slope | | | | | | | | | | |
| Rise time | | 35 | - | 65 | 35 | - | 65 | 35 | - | 65 | ps |
| Fall time | | 35 | - | 65 | 35 | - | 65 | 35 | - | 65 | ps |
| Intra differential pair skew | $V_{OD} = 800$ mV | - | - | 15 | - | - | 15 | - | - | 15 | ps |
| Intra-transceiver block skew (x4) | | - | - | 100 | - | - | 100 | - | - | 100 | ps |
| Inter-transceiver block skew (x8) | | - | - | 300 | - | - | 300 | - | - | 300 | ps |
| TXPLL (TXPLL0 and TXPLL1) | | | | | | | | | | | |
| VCO frequency range (low gear) | | 500 | - | 1562.5 | 500 | - | 1562.5 | 500 | - | 1562.5 | MHz |
| VCO frequency range (high gear) | | 1562.5 | | 3187.5 | 1562.5 | | 2500 | 1562.5 | - | 2125 | MHz |

Table 4–6. Stratix II GX Transceiver Block AC Specification (Part 6 of 6)

| Symbol / Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|--|------------|------------------------------------|-----|-----|--|-----|-----|---------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Bandwidth at 6.375 Gbps | BW = Low | - | 2 | - | - | - | - | - | - | - | MHz |
| | BW = Med | - | 3 | - | - | - | - | - | - | - | MHz |
| | BW = High | - | 7 | - | - | - | - | - | - | - | MHz |
| Bandwidth at 3.125 Gbps | BW = Low | - | 3 | - | - | 3 | - | - | 3 | - | MHz |
| | BW = Med | - | 5 | - | - | 5 | - | - | 5 | - | MHz |
| | BW = High | - | 9 | - | - | 9 | - | - | 9 | - | MHz |
| Bandwidth at 2.5 Gbps | BW = Low | - | 1 | - | - | 1 | - | - | 1 | - | MHz |
| | BW = Med | - | 2 | - | - | 2 | -- | - | 2 | - | MHz |
| | BW = High | - | 4 | - | - | 4 | - | - | 4 | - | MHz |
| TX PLL lock time from <code>gxb_powerdown</code> deassertion (9), (10) | | - | - | 100 | - | - | 100 | - | - | 100 | us |
| PLD-Transceiver Interface | | | | | | | | | | | |
| Interface speed | | 25 | - | 250 | 25 | - | 250 | 25 | - | 200 | MHz |
| Digital Reset Pulse Width | | Minimum is 2 parallel clock cycles | | | | | | | | | |

Notes to Table 4–6:

- (1) The device cannot tolerate prolonged operation at this absolute maximum. Refer to Figure 4–5 for more information.
- (2) The rate matcher supports only up to +/-300 ppm.
- (3) This parameter is measured by embedding the run length data in a PRBS sequence.
- (4) This feature is only available in PCI-Express (PIPE) mode.
- (5) Time taken to `rx_pll_locked` goes high from `rx_analogreset` deassertion. Refer to Figure 4–1.
- (6) This is how long GXB needs to stay in LTR mode after `rx_pll_locked` is asserted and before `rx_locktodata` is asserted in manual mode. Refer to Figure 4–1.
- (7) Time taken to recover valid data from GXB after `rx_locktodata` signal is asserted in manual mode. Measurement results are based on PRBS31, for native data rates only. Refer to Figure 4–1.
- (8) Time taken to recover valid data from GXB after `rx_freqlocked` signal goes high in automatic mode. Measurement results are based on PRBS31, for native data rates only. Refer to Figure 4–1.
- (9) Please refer to the Protocol Characterization documents for lock times specific to the protocols.
- (10) Time taken to lock TX PLL from `gxb_powerdown` deassertion.
- (11) The 1.2 V RX V_{ICM} setting is intended for DC-coupled LVDS links.
- (12) For AC-coupled links, the on-chip biasing circuit is switched off before and during configuration. Make sure that input specifications are not violated during this period.

Figure 4-1 shows the lock time parameters in manual mode, Figure 4-2 shows the lock time parameters in automatic mode.



LTD = Lock to data

LTR = Lock to reference clock

Figure 4-1. Lock Time Parameters for Manual Mode

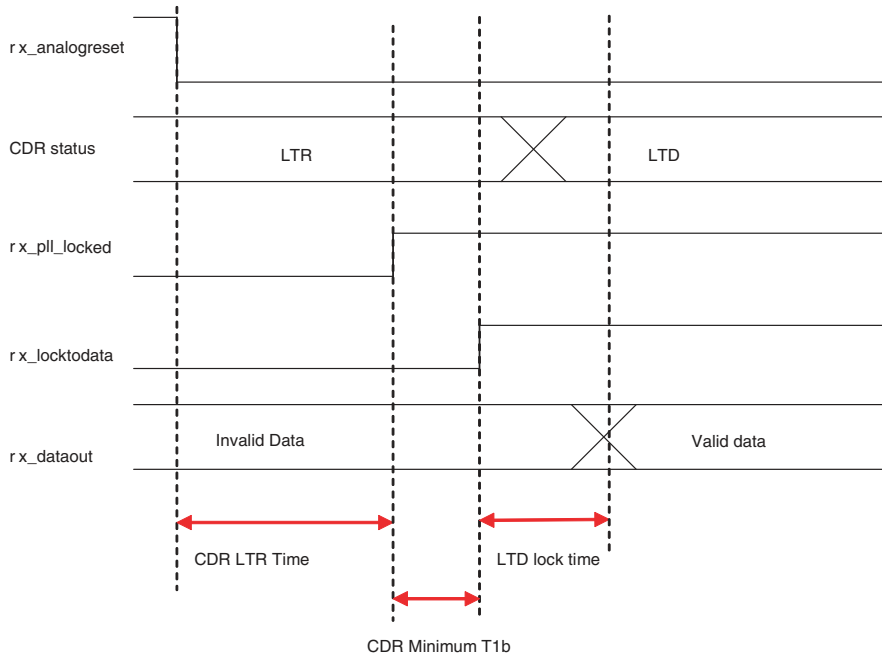
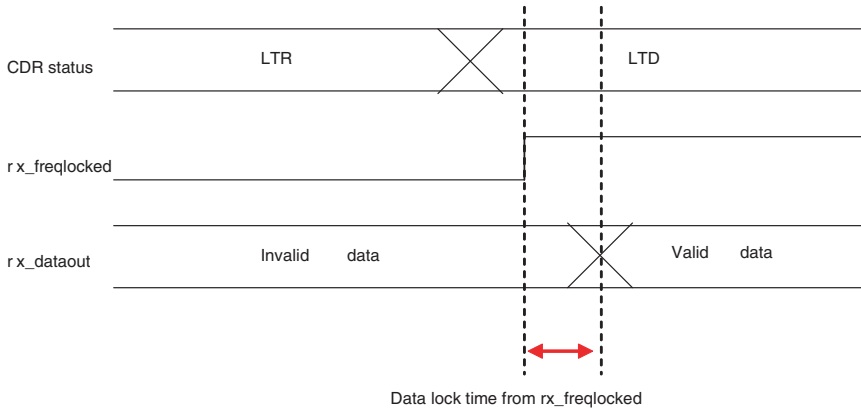


Figure 4–2. Lock Time Parameters for Automatic Mode



Figures 4–3 and 4–4 show differential receiver input and transmitter output waveforms, respectively.

Figure 4–3. Receiver Input Waveform

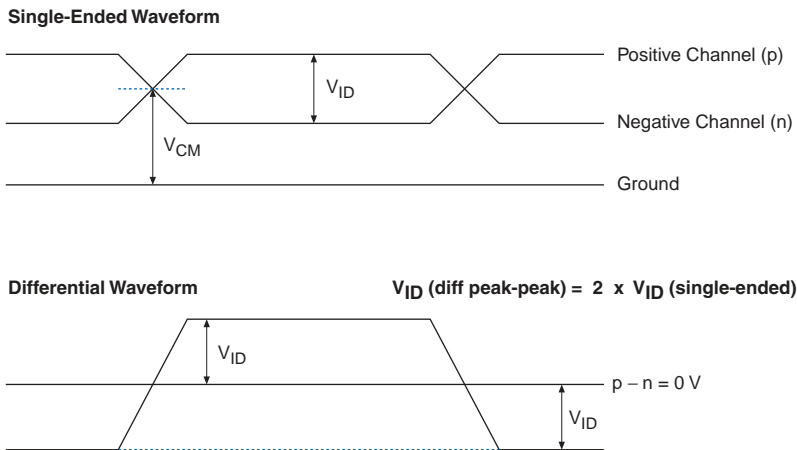


Figure 4–4. Transmitter Output Waveform

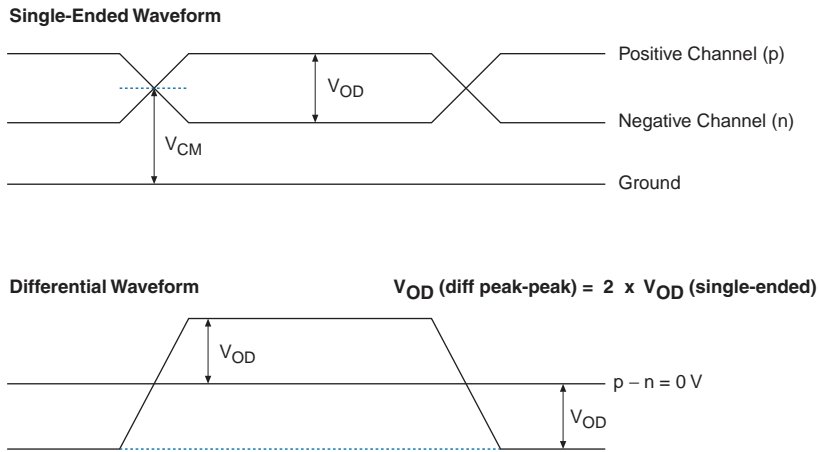
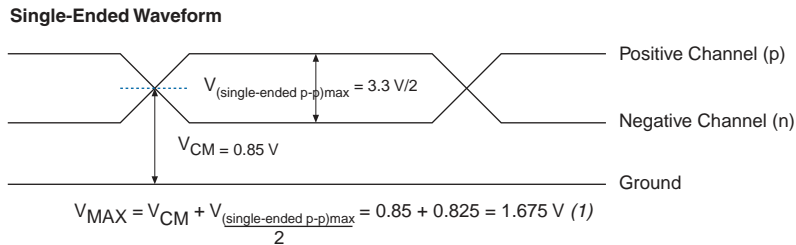


Figure 4–5. Maximum Receiver Input Pin Voltage



Note to Figure 4–5:

- (1) The absolute V_{MAX} that the receiver input pins can tolerate is 2 V.

Tables 4–7 through 4–12 show the typical V_{OD} for data rates from 600 Mbps to 6.375 Gbps. The specification is for measurement at the package ball.

| Table 4–7. Typical V_{OD} Setting, TX Term = 100 Ω Note (1) | | | | | | | |
|---|---|------------|------------|------------|-------------|-------------|-------------|
| V_{CCH} TX = 1.5 V | V_{OD} Setting (mV) | | | | | | |
| | 200 | 400 | 600 | 800 | 1000 | 1200 | 1400 |
| V_{OD} Typical (mV) | 220 | 430 | 625 | 830 | 1020 | 1200 | 1350 |

Note to Table 4–7:

- (1) Applicable to data rates from 600 Mbps to 6.375 Gbps. Specification is for measurement at the package ball.

| Table 4–8. Typical V_{OD} Setting, TX Term = 120 Ω Note (1) | | | | | |
|---|---|------------|------------|------------|-------------|
| V_{CCH} TX = 1.5 V | V_{OD} Setting (mV) | | | | |
| | 240 | 480 | 720 | 960 | 1200 |
| V_{OD} Typical (mV) | 260 | 510 | 750 | 975 | 1200 |

Note to Table 4–8:

- (1) Applicable to data rates from 600 Mbps to 6.375 Gbps. Specification is for measurement at the package ball.

| Table 4–9. Typical V_{OD} Setting, TX Term = 150 Ω Note (1) | | | | | |
|---|---|------------|------------|-------------|--|
| V_{CCH} TX = 1.5 V | V_{OD} Setting (mV) | | | | |
| | 300 | 600 | 900 | 1200 | |
| V_{OD} Typical (mV) | 325 | 625 | 920 | 1200 | |

Note to Table 4–9:

- (1) Applicable to data rates from 600 Mbps to 6.375 Gbps. Specification is for measurement at the package ball.

| Table 4–10. Typical V_{OD} Setting, TX Term = 100 Ω Note (1) | | | | | |
|--|---|------------|------------|------------|------------|
| V_{CCH} TX = 1.2 V | V_{OD} Setting (mV) | | | | |
| | 320 | 480 | 640 | 800 | 960 |
| V_{OD} Typical (mV) | 344 | 500 | 664 | 816 | 960 |

Note to Table 4–10:

- (1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

Table 4–11. Typical V_{OD} Setting, TX Term = 120 Ω Note (1)

| V_{CCH} TX = 1.2 V | V_{OD} Setting (mV) | | | | |
|-----------------------|-----------------------|-----|-----|-----|-----|
| | 192 | 384 | 576 | 768 | 960 |
| V_{OD} Typical (mV) | 210 | 410 | 600 | 780 | 960 |

Note to Table 4–11:

- (1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

Table 4–12. Typical V_{OD} Setting, TX Term = 150 Ω Note (1)

| V_{CCH} TX = 1.2 V | V_{OD} Setting (mV) | | | |
|-----------------------|-----------------------|-----|-----|-----|
| | 240 | 480 | 720 | 960 |
| V_{OD} Typical (mV) | 260 | 500 | 730 | 960 |

Note to Table 4–12:

- (1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

Tables 4–13 through 4–18 show the typical first post-tap pre-emphasis.

Table 4–13. Typical Pre-Emphasis (First Post-Tap), Note (1) (Part 1 of 2)

| V_{CCH} TX = 1.5 V | First Post Tap Pre-Emphasis Level | | | | | | | | | | | |
|--|-----------------------------------|-----|------|------|------|------|------|------|------|------|------|------|
| | V_{OD} Setting (mV) | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
| TX Term = 100 Ω | | | | | | | | | | | | |
| 400 | 24% | 62% | 112% | 184% | | | | | | | | |
| 600 | | 31% | 56% | 86% | 122% | 168% | 230% | 329% | 457% | | | |
| 800 | | 20% | 35% | 53% | 73% | 96% | 123% | 156% | 196% | 237% | 312% | 387% |
| 1000 | | | 23% | 36% | 49% | 64% | 79% | 97% | 118% | 141% | 165% | 200% |
| 1200 | | | 17% | 25% | 35% | 45% | 56% | 68% | 82% | 95% | 110% | 125% |

Table 4–13. Typical Pre-Emphasis (First Post-Tap), Note (1) (Part 2 of 2)

| $V_{CCH\ TX}$ = 1.5 V | First Post Tap Pre-Emphasis Level | | | | | | | | | | | |
|-----------------------------|-----------------------------------|---|---|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| V_{OD} Setting (mV) | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
| 1400 | | | | 20% | 26% | 33% | 41% | 51% | 58% | 67% | 77% | 86% |

Note to Table 4–13:

- (1) Applicable to data rates from 600 Mbps to 6.375 Gbps. Specification is for measurement at the package ball.

Table 4–14. Typical Pre-Emphasis (First Post-Tap), Note (1)

| $V_{CCH\ TX}$ = 1.5 V | First Post Tap Pre-Emphasis Level | | | | | | | | | | | |
|--|-----------------------------------|-----|-----|------|------|------|------|------|------|------|------|------|
| V_{OD} Setting (mV) | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
| TX Term = 120 Ω | | | | | | | | | | | | |
| 240 | 45% | | | | | | | | | | | |
| 480 | | 41% | 76% | 114% | 166% | 257% | 355% | | | | | |
| 720 | | 23% | 38% | 55% | 84% | 108% | 137% | 179% | 226% | 280% | 405% | 477% |
| 960 | | 15% | 24% | 36% | 47% | 64% | 80% | 97% | 122% | 140% | 170% | 196% |
| 1200 | | | 18% | 22% | 30% | 41% | 51% | 63% | 77% | 86% | 98% | 116% |

Note to Table 4–14:

- (1) Applicable to data rates from 600 Mbps to 6.375 Gbps. Specification is for measurement at the package ball.

Table 4–15. Typical Pre-Emphasis (First Post-Tap), Note (1) (Part 1 of 2)

| $V_{CCH\ TX}$ = 1.5 V | First Post Tap Pre-Emphasis Level | | | | | | | | | | | |
|--|-----------------------------------|-----|---|---|---|---|---|---|---|----|----|----|
| V_{OD} Setting (mV) | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
| TX Term = 150 Ω | | | | | | | | | | | | |
| 300 | 32% | 85% | | | | | | | | | | |

Table 4–15. Typical Pre-Emphasis (First Post-Tap), Note (1) (Part 2 of 2)

| $V_{CCH\ TX} = 1.5\ V$ | First Post Tap Pre-Emphasis Level | | | | | | | | | | | |
|------------------------|-----------------------------------|-----|-----|-----|------|------|------|------|------|------|------|------|
| V_{OD} Setting (mV) | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
| 600 | | 33% | 53% | 80% | 115% | 157% | 195% | 294% | 386% | | | |
| 900 | | 19% | 28% | 38% | 56% | 70% | 86% | 113% | 133% | 168% | 196% | 242% |
| 1200 | | | 17% | 22% | 31% | 40% | 52% | 62% | 75% | 86% | 96% | 112% |

Note to Table 4–15:

(1) Applicable to data rates from 600 Mbps to 6.375 Gbps. Specification is for measurement at the package ball.

Table 4–16. Typical Pre-Emphasis (First Post-Tap), Note (1)

| $V_{CCH\ TX} = 1.2\ V$ | First Post Tap Pre-Emphasis Level | | | | | | | | | | | |
|------------------------|--|-----|------|-----|------|------|------|------|------|------|------|------|
| V_{OD} Setting (mV) | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
| | TX Term = 100 Ω | | | | | | | | | | | |
| 320 | 24% | 61% | 114% | | | | | | | | | |
| 480 | | 31% | 55% | 86% | 121% | 170% | 232% | 333% | | | | |
| 640 | | 20% | 35% | 54% | 72% | 95% | 124% | 157% | 195% | 233% | 307% | 373% |
| 800 | | | 23% | 36% | 49% | 64% | 81% | 97% | 117% | 140% | 161% | 195% |
| 960 | | | 18% | 25% | 35% | 44% | 57% | 69% | 82% | 94% | 108% | 127% |

Note to Table 4–16:

(1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

Table 4-17. Typical Pre-Emphasis (First Post-Tap), Note (1)

| $V_{CCH\ TX}$ = 1.2 V | First Post Tap Pre-Emphasis Level | | | | | | | | | | | |
|-----------------------------|--|-----|-----|------|------|------|------|------|------|------|------|------|
| V_{OD} Setting (mV) | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
| | TX Term = 120 Ω | | | | | | | | | | | |
| 192 | 45% | | | | | | | | | | | |
| 384 | | 41% | 76% | 114% | 166% | 257% | 355% | | | | | |
| 576 | | 23% | 38% | 55% | 84% | 108% | 137% | 179% | 226% | 280% | 405% | 477% |
| 768 | | 15% | 24% | 36% | 47% | 64% | 80% | 97% | 122% | 140% | 170% | 196% |
| 960 | | | 18% | 22% | 30% | 41% | 51% | 63% | 77% | 86% | 98% | 116% |

Note to Table 4-17:

- (1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

Table 4-18. Typical Pre-Emphasis (First Post-Tap), Note (1)

| $V_{CCH\ TX}$ = 1.2 V | First Post Tap Pre-Emphasis Level | | | | | | | | | | | |
|-----------------------------|--|-----|-----|-----|------|------|------|------|------|------|------|------|
| V_{OD} Setting (mV) | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
| | TX Term = 150 Ω | | | | | | | | | | | |
| 240 | 31% | 85% | | | | | | | | | | |
| 480 | | 32% | 52% | 78% | 112% | 152% | 195% | 275% | | | | |
| 720 | | 19% | 28% | 37% | 56% | 68% | 86% | 108% | 133% | 169% | 194% | 239% |
| 960 | | | 17% | 22% | 30% | 39% | 51% | 59% | 75% | 85% | 94% | 109% |

Note to Table 4-18:

- (1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

Table 4–19 shows the Stratix II GX transceiver block AC specifications.

| Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 1 of 19) | | | | | | | | | | | |
|--|---|---------------------------------------|-----|------|---|-----|------|---------------------------------------|-----|------|------|
| Symbol/ Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| SONET/SDH Transmit Jitter Generation (7) | | | | | | | | | | | |
| Peak-to-peak jitter at 622.08 Mbps | REFCLK = 77.76 MHz Pattern = PRBS23 V _{OD} = 800 mV No Pre-emphasis | - | - | 0.1 | - | - | 0.1 | - | - | 0.1 | UI |
| RMS jitter at 622.08 Mbps | REFCLK = 77.76 MHz Pattern = PRBS23 V _{OD} = 800 mV No Pre-emphasis | - | - | 0.01 | - | - | 0.01 | - | - | 0.01 | UI |
| Peak-to-peak jitter at 2488.32 Mbps | REFCLK = 155.52 MHz Pattern = PRBS23 V _{OD} = 800 mV No Pre-emphasis | - | - | 0.1 | - | - | 0.1 | - | - | 0.1 | UI |
| RMS jitter at 2488.32 Mbps | REFCLK = 155.52 MHz Pattern = PRBS23 V _{OD} = 800 mV No Pre-emphasis | - | - | 0.01 | - | - | 0.01 | - | - | 0.01 | UI |

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 2 of 19)

| Symbol/ Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|--|---|---------------------------------------|-----|-----|---|-----|-----|---------------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| SONET/SDH Receiver Jitter Tolerance (7) | | | | | | | | | | | |
| Jitter tolerance at 622.08 Mbps | Jitter frequency = 0.03 KHz Pattern = PRBS23 No Equalization DC Gain = 0 dB | > 15 | | | > 15 | | | > 15 | | | UI |
| | Jitter frequency = 25 KHz Pattern = PRBS23 No Equalization DC Gain = 0 dB | > 1.5 | | | > 1.5 | | | > 1.5 | | | UI |
| | Jitter frequency = 250 KHz Pattern = PRBS23 No Equalization DC Gain = 0 dB | > 0.15 | | | > 0.15 | | | > 0.15 | | | UI |
| Jitter tolerance at 2488.32 MBps | Jitter frequency = 0.06 KHz Pattern = PRBS23 No Equalization DC Gain = 0 dB | > 15 | | | > 15 | | | > 15 | | | UI |
| | Jitter frequency = 100 KHz Pattern = PRBS23 No Equalization DC Gain = 0 dB | > 1.5 | | | > 1.5 | | | > 1.5 | | | UI |
| | Jitter frequency = 1 MHz Pattern = PRBS23 No Equalization DC Gain = 0 dB | > 0.15 | | | > 0.15 | | | > 0.15 | | | UI |
| | Jitter frequency = 10 MHz Pattern = PRBS23 No Equalization DC Gain = 0 dB | > 0.15 | | | > 0.15 | | | > 0.15 | | | UI |

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 3 of 19)

| Symbol/ Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|---|--|---------------------------------------|-----|------|---|-----|------|---------------------------------------|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Fibre Channel Transmit Jitter Generation (8), (17) | | | | | | | | | | | |
| Total jitter FC-1 | REFCLK = 106.25 MHz Pattern = CRPAT V _{OD} = 800 mV No Pre-emphasis | - | - | 0.23 | - | - | 0.23 | - | - | 0.23 | UI |
| Deterministic jitter FC-1 | REFCLK = 106.25 MHz Pattern = CRPAT V _{OD} = 800 mV No Pre-emphasis | - | - | 0.11 | - | - | 0.11 | - | - | 0.11 | UI |
| Total jitter FC-2 | REFCLK = 106.25 MHz Pattern = CRPAT V _{OD} = 800 mV No Pre-emphasis | - | - | 0.33 | - | - | 0.33 | - | - | 0.33 | UI |
| Deterministic jitter FC-2 | REFCLK = 106.25 MHz Pattern = CRPAT V _{OD} = 800 mV No Pre-emphasis | - | - | 0.2 | - | - | 0.2 | - | - | 0.2 | UI |
| Total jitter FC-4 | REFCLK = 106.25 MHz Pattern = CRPAT V _{OD} = 800 mV No Pre-emphasis | - | - | 0.52 | - | - | 0.52 | - | - | 0.52 | UI |
| Deterministic jitter FC-4 | REFCLK = 106.25 MHz Pattern = CRPAT V _{OD} = 800 mV No Pre-emphasis | - | - | 0.33 | - | - | 0.33 | - | - | 0.33 | UI |
| Fibre Channel Receiver Jitter Tolerance (8), (18) | | | | | | | | | | | |
| Deterministic jitter FC-1 | Pattern = CJTPAT No Equalization DC Gain = 0 dB | > 0.37 | | | > 0.37 | | | > 0.37 | | | UI |
| Random jitter FC- 1 | Pattern = CJTPAT No Equalization DC Gain = 0 dB | > 0.31 | | | > 0.31 | | | > 0.31 | | | UI |

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 4 of 19)

| Symbol/ Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|--|---|---------------------------------------|-----|------|---|-----|------|---------------------------------------|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Sinusoidal jitter FC-1 | Fc/25000 | > 1.5 | | | > 1.5 | | | > 1.5 | | | UI |
| | Fc/1667 | > 0.1 | | | > 0.1 | | | > 0.1 | | | UI |
| Deterministic jitter FC-2 | Pattern = CJTPAT No Equalization DC Gain = 0 dB | > 0.33 | | | > 0.33 | | | > 0.33 | | | UI |
| Random jitter FC- 2 | Pattern = CJTPAT No Equalization DC Gain = 0 dB | > 0.29 | | | > 0.29 | | | > 0.29 | | | UI |
| Sinusoidal jitter FC-2 | Fc/25000 | > 1.5 | | | > 1.5 | | | > 1.5 | | | UI |
| | Fc/1667 | > 0.1 | | | > 0.1 | | | > 0.1 | | | UI |
| Deterministic jitter FC-4 | Pattern = CJTPAT No Equalization DC Gain = 0 dB | > 0.33 | | | > 0.33 | | | > 0.33 | | | UI |
| Random jitter FC- 4 | Pattern = CJTPAT No Equalization DC Gain = 0 dB | > 0.29 | | | > 0.29 | | | > 0.29 | | | UI |
| Sinusoidal jitter FC-4 | Fc/25000 | > 1.5 | | | > 1.5 | | | > 1.5 | | | UI |
| | Fc/1667 | > 0.1 | | | > 0.1 | | | > 0.1 | | | UI |
| XAUI Transmit Jitter Generation (9) | | | | | | | | | | | |
| Total jitter at 3.125 Gbps | REFCLK = 156.25 MHz Pattern = CJPAT V _{OD} = 1200 mV No Pre-emphasis | - | - | 0.3 | - | - | 0.3 | - | - | 0.3 | UI |
| Deterministic jitter at 3.125 Gbps | REFCLK = 156.25 MHz Pattern = CJPAT V _{OD} = 1200 mV No Pre-emphasis | - | - | 0.17 | - | - | 0.17 | - | - | 0.17 | UI |
| XAUI Receiver Jitter Tolerance (9) | | | | | | | | | | | |
| Total jitter | Pattern = CJPAT No Equalization DC Gain = 3 dB | > 0.65 | | | > 0.65 | | | > 0.65 | | | UI |
| Deterministic jitter | Pattern = CJPAT No Equalization DC Gain = 3 dB | > 0.37 | | | > 0.37 | | | > 0.37 | | | UI |

| Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 5 of 19) | | | | | | | | | | | |
|--|--|---------------------------------------|-----|------|---|-----|------|---------------------------------------|-----|------|------|
| Symbol/ Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Peak-to-peak jitter | Jitter frequency = 22.1 KHz | > 8.5 | | | > 8.5 | | | > 8.5 | | | UI |
| Peak-to-peak jitter | Jitter frequency = 1.875 MHz | > 0.1 | | | > 0.1 | | | > 0.1 | | | UI |
| Peak-to-peak jitter | Jitter frequency = 20 MHz | > 0.1 | | | > 0.1 | | | > 0.1 | | | UI |
| PCI Express Transmit Jitter Generation (10) | | | | | | | | | | | |
| Total jitter at 2.5 Gbps | Compliance pattern V _{OD} = 800 mV Pre-emphasis (1st post-tap) = Setting 5 | - | - | 0.25 | - | - | 0.25 | - | - | 0.25 | UI |
| PCI Express Receiver Jitter Tolerance (10) | | | | | | | | | | | |
| Total jitter at 2.5 Gbps | Compliance pattern No Equalization DC gain = 3 dB | > 0.6 | | | > 0.6 | | | > 0.6 | | | UI |
| Serial RapidIO Transmit Jitter Generation (11) | | | | | | | | | | | |
| Deterministic Jitter (peak-to-peak) | Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT V _{OD} = 800 mV No Pre-emphasis | - | - | 0.17 | - | - | 0.17 | - | - | 0.17 | UI |
| Total Jitter (peak-to-peak) | Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT V _{OD} = 800 mV No Pre-emphasis | - | - | 0.35 | - | - | 0.35 | - | - | 0.35 | UI |

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 6 of 19)

| Symbol/ Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|---|---|---------------------------------------|-----|-----|---|-----|-----|---------------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Serial RapidIO Receiver Jitter Tolerance (11) | | | | | | | | | | | |
| Deterministic Jitter Tolerance (peak-to-peak) | Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT Equalizer Setting = 0 for 1.25 Gbps Equalizer Setting = 6 for 2.5 Gbps Equalizer Setting = 6 for 3.125 Gbps | > 0.37 | | | > 0.37 | | | > 0.37 | | | UI |
| Combined Deterministic and Random Jitter Tolerance (peak-to-peak) | Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT Equalizer Setting = 0 for 1.25 Gbps Equalizer Setting = 6 for 2.5 Gbps Equalizer Setting = 6 for 3.125 Gbps | > 0.55 | | | > 0.55 | | | > 0.55 | | | UI |

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 7 of 19)

| Symbol/ Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|--|--|---------------------------------------|-----|-----|---|-----|-----|---------------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Sinusoidal Jitter Tolerance (peak-to-peak) | Jitter Frequency = 22.1 KHz Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT Equalizer Setting = 0 for 1.25 Gbps Equalizer Setting = 6 for 2.5 Gbps Equalizer Setting = 6 for 3.125 Gbps | > 8.5 | | | > 8.5 | | | > 8.5 | | | UI |
| | Jitter Frequency = 1.875 MHz Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT Equalizer Setting = 0 for 1.25 Gbps Equalizer Setting = 6 for 2.5 Gbps Equalizer Setting = 6 for 3.125 Gbps | > 0.1 | | | > 0.1 | | | > 0.1 | | | UI |
| | Jitter Frequency = 20 MHz Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT Equalizer Setting = 0 for 1.25 Gbps Equalizer Setting = 6 for 2.5 Gbps Equalizer Setting = 6 for 3.125 Gbps | > 0.1 | | | > 0.1 | | | > 0.1 | | | UI |

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 8 of 19)

| Symbol/ Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|---|--|---------------------------------------|-----|-------|---|-----|-------|---------------------------------------|-----|-------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| GIGE Transmit Jitter Generation (12) | | | | | | | | | | | |
| Deterministic Jitter (peak-to-peak) | Data Rate = 1.25 Gbps REFCLK = 125 MHz Pattern = CRPAT V _{OD} = 1400 mV No Pre-emphasis | - | - | 0.14 | - | - | 0.14 | - | - | 0.14 | UI |
| Total Jitter (peak-to-peak) | Data Rate = 1.25 Gbps REFCLK = 125 MHz Pattern = CRPAT V _{OD} = 1400 mV No Pre-emphasis | - | - | 0.279 | - | - | 0.279 | - | - | 0.279 | UI |
| GIGE Receiver Jitter Tolerance (12) | | | | | | | | | | | |
| Deterministic Jitter Tolerance (peak-to-peak) | Data Rate = 1.25 Gbps REFCLK = 125 MHz Pattern = CJPAT No Equalization | > 0.4 | | | > 0.4 | | | > 0.4 | | | UI |
| Combined Deterministic and Random Jitter Tolerance (peak-to-peak) | Data Rate = 1.25 Gbps REFCLK = 125 MHz Pattern = CJPAT No Equalization | > 0.66 | | | > 0.66 | | | > 0.66 | | | UI |
| HiGig Transmit Jitter Generation (4), (13) | | | | | | | | | | | |
| Deterministic Jitter (peak-to-peak) | Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT V _{OD} = 1200 mV No Pre-emphasis | - | - | 0.17 | - | | | - | | | UI |
| Total Jitter (peak-to-peak) | Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT V _{OD} = 1200 mV No Pre-emphasis | - | - | 0.35 | - | | | - | | | UI |

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 9 of 19)

| Symbol/ Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|---|---|---------------------------------------|-----|-----|---|-----|-----|---------------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| HiGig Receiver Jitter Tolerance (13) | | | | | | | | | | | |
| Deterministic Jitter Tolerance (peak-to-peak) | Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT No Equalization DC Gain = 3 dB | > 0.37 | | | - | | | - | | | UI |
| Combined Deterministic and Random Jitter Tolerance (peak-to-peak) | Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT No Equalization DC Gain = 3 dB | > 0.65 | | | - | | | - | | | UI |
| | Jitter Frequency = 22.1 KHz Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT No Equalization DC Gain = 3 dB | > 8.5 | | | - | | | - | | | UI |

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 10 of 19)

| Symbol/ Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|---|--|---------------------------------------|-----|-----|---|-----|-----|---------------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Sinusoidal Jitter Tolerance (peak-to-peak) | Jitter Frequency = 1.875 MHz Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT No Equalization DC Gain = 3 dB | > 0.1 | | | - | | | - | | | UI |
| | Jitter Frequency = 20 MHz Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT No Equalization DC Gain = 3 dB | > 0.1 | | | - | | | - | | | UI |
| (OIF) CEI Transmitter Jitter Generation (14) | | | | | | | | | | | |
| Total Jitter (peak-to-peak) | Data Rate = 6.375 Gbps REFCLK = 318.75 MHz Pattern = PRBS15 Vod=1000 mV (5) NoPre-emphasis BER = 10 ⁻¹² | | | 0.3 | | | N/A | | | N/A | UI |
| (OIF) CEI Receiver Jitter Tolerance (14) | | | | | | | | | | | |
| Deterministic Jitter Tolerance (peak-to-peak) | Data Rate = 6.375 Gbps Pattern = PRBS31 Equalizer Setting = 15 DCGain = 0 dB BER = 10 ⁻¹² | > 0.675 | | | N/A | | | N/A | | | UI |

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 11 of 19)

| Symbol/ Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|---|--|---------------------------------------|-----|-----|---|-----|-----|---------------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Combined Deterministic and Random Jitter Tolerance (peak-to-peak) | Data Rate = 6.375 Gbps Pattern = PRBS31 Equalizer Setting = 15 DCGain = 0 dB BER = 10 ⁻¹² | > 0.988 | | | N/A | | | N/A | | | UI |
| Sinusoidal Jitter Tolerance (peak-to-peak) | Jitter Frequency = 38.2 KHz Data Rate = 6.375 Gbps Pattern = PRBS31 Equalizer Setting = 15 DCGain = 0 dB BER = 10 ⁻¹² | > 5 | | | N/A | | | N/A | | | UI |
| | Jitter Frequency = 3.82 MHz Data Rate=6.375 Gbps Pattern = PRBS31 Equalizer Setting = 15 DCGain = 0 dB BER = 10 ⁻¹² | > 0.05 | | | N/A | | | N/A | | | UI |
| | Jitter Frequency = 20 MHz Data Rate = 6.375 Gbps Pattern = PRBS31 Equalizer Setting = 15 DCGain = 0 dB BER = 10 ⁻¹² | > 0.05 | | | N/A | | | N/A | | | UI |

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 12 of 19)

| Symbol/ Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|--|---|---------------------------------------|-----|-------|---|-----|-------|---------------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| CPRI Transmitter Jitter Generation (15) | | | | | | | | | | | |
| Deterministic Jitter (peak-to-peak) | Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps REFCLK = 61.44 MHz for 614.4 Mbps and 1.2288 Gbps REFCLK = 122.88 MHz for 2.4576 Gbps Pattern = CJPAT Vod = 1400 mV No Pre-emphasis | | | 0.14 | | | 0.14 | | | N/A | UI |
| Total Jitter (peak-to-peak) | Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps REFCLK = 61.44 MHz for 614.4 Mbps and 1.2288 Gbps REFCLK = 122.88 MHz for 2.4576 Gbps Pattern = CJPAT Vod = 1400 mV No Pre-emphasis | | | 0.279 | | | 0.279 | | | N/A | UI |

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 13 of 19)

| Symbol/ Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|---|---|---------------------------------------|-----|-----|---|-----|-----|---------------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| CPRI Receiver Jitter Tolerance (15) | | | | | | | | | | | |
| Deterministic Jitter Tolerance (peak-to-peak) | Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps REFCLK = 61.44 MHz for 614.4 Mbps REFCLK = 122.88 MHz for 1.2288 Gbps and 2.4576 Gbps Pattern = CJPAT Equalizer Setting = 6 DC Gain = 0 dB | > 0.4 | | | > 0.4 | | | N/A | | | UI |
| Combined Deterministic and Random Jitter Tolerance (peak-to-peak) | Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps REFCLK = 61.44 MHz for 614.4 Mbps REFCLK = 122.88 MHz for 1.2288 Gbps and 2.4576 Gbps Pattern = CJPAT Equalizer Setting = 6 DC Gain = 0 dB | > 0.66 | | | > 0.66 | | | N/A | | | UI |

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 14 of 19)

| Symbol/ Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|--|---|---------------------------------------|-----|-----|---|-----|-----|---------------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Sinusoidal Jitter Tolerance (peak-to-peak) (6) | Jitter Frequency = 22.1 KHz Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps REFCLK = 61.44 MHz for 614.4 Mbps REFCLK = 122.88 MHz for 1.2288 Gbps and 2.4576 Gbps Pattern = CJPAT Equalizer Setting = 6 DC Gain = 0 dB | > 8.5 | | | > 8.5 | | | N/A | | | UI |
| | Jitter Frequency = 1.875MHz Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps REFCLK = 61.44 MHz for 614.4 Mbps REFCLK = 122.88 MHz for 1.2288 Gbps and 2.4576 Gbps Pattern = CJPAT Equalizer Setting = 6 DC Gain = 0 dB | > 0.1 | | | > 0.1 | | | N/A | | | UI |

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 15 of 19)

| Symbol/ Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|---|---|---------------------------------------|-------|-----|---|-------|-----|---------------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Sinusoidal Jitter Tolerance (peak-to-peak) (6) (cont.) | Jitter Frequency = 20 MHz Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps REFCLK = 61.44 MHz for 614.4 Mbps REFCLK = 122.88 MHz for 1.2288 Gbps and 2.4576 Gbps Pattern = CJPAT Equalizer Setting = 6 DC Gain = 0 dB | | > 0.1 | | | > 0.1 | | | N/A | | UI |

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 16 of 19)

| Symbol/ Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|---|---|---------------------------------------|-----|-----|---|-----|-----|---------------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| SDI Transmitter Jitter Generation (16) | | | | | | | | | | | |
| Alignment Jitter (peak-to-peak) | Data Rate = 1.485 Gbps (HD) REFCLK = 74.25 MHz Pattern = ColorBar Vod = 800 mV No Pre-emphasis Low-Frequency Roll-Off = 100 KHz | 0.2 | | | 0.2 | | | 0.2 | | | UI |
| | Data Rate = 2.97 Gbps (3G) REFCLK = 148.5 MHz Pattern = ColorBar Vod = 800 mV No Pre-emphasis Low-Frequency Roll-Off = 100 KHz | 0.3 | | | 0.3 | | | 0.3 | | | UI |

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 17 of 19)

| Symbol/ Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|--|--|---------------------------------------|-----|-----|---|-----|-----|---------------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| SDI Receiver Jitter Tolerance (16) | | | | | | | | | | | |
| Sinusoidal Jitter Tolerance (peak-to-peak) | Jitter Frequency = 15 KHz Data Rate = 2.97 Gbps (3G) REFCLK = 148.5 MHz Pattern = Single Line Scramble Color Bar No Equalization DC Gain = 0 dB | > 2 | | | > 2 | | | > 2 | | | UI |
| | Jitter Frequency = 100 KHz Data Rate = 2.97 Gbps (3G) REFCLK = 148.5 MHz Pattern = Single Line Scramble Color Bar No Equalization DC Gain = 0 dB | > 0.3 | | | > 0.3 | | | > 0.3 | | | UI |
| | Jitter Frequency = 148.5 MHz Data Rate = 2.97 Gbps (3G) REFCLK = 148.5 MHz Pattern = Single Line Scramble Color Bar No Equalization DC Gain = 0 dB | > 0.3 | | | > 0.3 | | | > 0.3 | | | UI |

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 18 of 19)

| Symbol/ Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|--|---|---------------------------------------|-----|-----|---|-----|-----|---------------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Sinusoidal Jitter Tolerance (peak-to-peak) | Jitter Frequency = 20 KHz Data Rate = 1.485 Gbps (HD) REFCLK = 74.25 MHz Pattern = 75% Color Bar No Equalization DC Gain = 0 dB | > 1 | | | > 1 | | | > 1 | | | UI |
| | Jitter Frequency = 100 KHz Data Rate = 1.485 Gbps (HD) REFCLK = 74.25 MHz Pattern = 75% Color Bar No Equalization DC Gain = 0 dB | > 0.2 | | | > 0.2 | | | > 0.2 | | | UI |
| | Jitter Frequency = 148.5 MHz Data Rate = 1.485 Gbps (HD) REFCLK = 74.25 MHz Pattern = 75% Color Bar No Equalization DC Gain = 0 dB | > 0.2 | | | > 0.2 | | | > 0.2 | | | UI |

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 19 of 19)

| Symbol/ Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|------------------------|------------|---------------------------------------|-----|-----|---|-----|-----|---------------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |

Notes to Table 4–19:

- (1) Dedicated REFCLK pins were used to drive the input reference clocks.
- (2) Jitter numbers specified are valid for the stated conditions only.
- (3) Refer to the protocol characterization documents for detailed information.
- (4) HiGig configuration is available in a -3 speed grade only. For more information, refer to the *Stratix II GX Transceiver Architecture Overview* chapter in volume 2 of the *Stratix II GX Device Handbook*.
- (5) Stratix II GX transceivers meet CEI jitter generation specification of 0.3 UI for a V_{OD} range of 400 mV to 1000 mV.
- (6) The Sinusoidal Jitter Tolerance Mask is defined only for low voltage (LV) variant of CPRI.
- (7) The jitter numbers for SONET/SDH are compliant to the GR-253-CORE Issue 3 Specification.
- (8) The jitter numbers for Fibre Channel are compliant to the FC-PI-4 Specification revision 6.10.
- (9) The jitter numbers for XAUI are compliant to the IEEE802.3ae-2002 Specification.
- (10) The jitter numbers for PCI Express are compliant to the PCIe Base Specification 2.0.
- (11) The jitter numbers for Serial RapidIO are compliant to the RapidIO Specification 1.3.
- (12) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
- (13) The jitter numbers for HiGig are compliant to the IEEE802.3ae-2002 Specification.
- (14) The jitter numbers for (OIF) CEI are compliant to the OIF-CEI-02.0 Specification.
- (15) The jitter numbers for CPRI are compliant to the CPRI Specification V2.1.
- (16) The HD-SDI and 3G-SDI jitter numbers are compliant to the SMPTE292M and SMPTE424M Specifications.
- (17) The Fibre Channel transmitter jitter generation numbers are compliant to the specification at β_T interoperability point.
- (18) The Fibre Channel receiver jitter tolerance numbers are compliant to the specification at β_R interoperability point.

Table 4–20 provides information on recommended input clock jitter for each mode.

Table 4–20. Recommended Input Clock Jitter (Part 1 of 2)

| Mode | Reference Clock (MHz) | Vectron LVPECL XO Type/Model | Frequency Range (MHz) | RMS Jitter (12 kHz to 20 MHz) (ps) | Period Jitter (Peak to Peak) (ps) | Phase Noise at 1 MHz (dB c/Hz) |
|---------------|-----------------------|------------------------------|-----------------------|------------------------------------|-----------------------------------|--------------------------------|
| PCI-E | 100 | VCC6-Q/R | 10 to 270 | 0.3 | 23 | -149.9957 |
| (OIF) CEI PHY | 156.25 | VCC6-Q/R | 10 to 270 | 0.3 | 23 | -146.2169 |
| | 622.08 | VCC6-Q | 270 to 800 | 2 | 30 | Not available |
| GIGE | 62.5 | VCC6-Q/R | 10 to 270 | 0.3 | 23 | -149.9957 |
| | 125 | VCC6-Q/R | 10 to 270 | 0.3 | 23 | -146.9957 |
| XAUI | 156.25 | VCC6-Q/R | 10 to 270 | 0.3 | 23 | -146.2169 |

Table 4–20. Recommended Input Clock Jitter (Part 2 of 2)

| Mode | Reference Clock (MHz) | Vectron LVPECL XO Type/Model | Frequency Range (MHz) | RMS Jitter (12 kHz to 20 MHz) (ps) | Period Jitter (Peak to Peak) (ps) | Phase Noise at 1 MHz (dB c/Hz) |
|-----------------|-----------------------|------------------------------|-----------------------|------------------------------------|-----------------------------------|--------------------------------|
| SONET/SDH OC-48 | 77.76 | VCC6-Q/R | 10 to 270 | 0.3 | 23 | -149.5476 |
| | 155.52 | VCC6-Q/R | 10 to 270 | 0.3 | 23 | -149.1903 |
| | 311.04 | VCC6-Q | 270 to 800 | 2 | 30 | Not available |
| | 622.08 | VCC6-Q | 270 to 800 | 2 | 30 | Not available |
| SONET/SDH OC-12 | 62.2 | VCC6-Q/R | 10 to 270 | 0.3 | 23 | -149.6289 |
| | 311 | VCC6-Q | 270 to 800 | 2 | 30 | Not available |
| | 77.76 | VCC6-Q/R | 10 to 270 | 0.3 | 23 | -149.5476 |
| | 155.52 | VCC6-Q/R | 10 to 270 | 0.3 | 23 | -149.1903 |
| | 622.08 | VCC6-Q | 270 to 800 | 2 | 30 | Not available |

Tables 4–21 and 4–22 show the transmitter and receiver PCS latency for each mode, respectively.

Table 4–21. PCS Latency (Part 1 of 2) Note (1)

| Functional Mode | Configuration | Transmitter PCS Latency | | | | | Sum (2) |
|-----------------|------------------------------------|-------------------------|--------------------|-----------------|------------------|----------------|---------|
| | | TX PIPE | TX Phase Comp FIFO | Byte Serializer | TX State Machine | 8B/10B Encoder | |
| XAUI | | - | 2-3 | 1 | 0.5 | 0.5 | 4-5 |
| PIPE | ×1, ×4, ×8 8-bit channel width | 1 | 3-4 | 1 | - | 1 | 6-7 |
| | ×1, ×4, ×8 16-bit channel width | 1 | 3-4 | 1 | - | 0.5 | 6-7 |
| GIGE | | - | 2-3 | 1 | - | 1 | 4-5 |
| SONET/SDH | OC-12 | - | 2-3 | 1 | - | 1 | 4-5 |
| | OC-48 | - | 2-3 | 1 | - | 0.5 | 4-5 |
| | OC-96 | - | 2-3 | 1 | - | 0.5 | 4-5 |
| (OIF) CEI PHY | | - | 2-3 | 1 | - | 0.5 | 4-5 |
| CPRI (3) | 614 Mbps, 1.228 Gbps | - | 2 | 1 | - | 1 | 4 |
| | 2.456 Gbps | - | 2-3 | 1 | - | 1 | 4-5 |

| Table 4–21. PCS Latency (Part 2 of 2) Note (1) | | | | | | | |
|---|---------------------------------------|--------------------------------|---------------------------|------------------------|-------------------------|-----------------------|----------------|
| Functional Mode | Configuration | Transmitter PCS Latency | | | | | |
| | | TX PIPE | TX Phase Comp FIFO | Byte Serializer | TX State Machine | 8B/10B Encoder | Sum (2) |
| Serial RapidIO | 1.25 Gbps, 2.5 Gbps, 3.125 Gbps | - | 2-3 | 1 | - | 0.5 | 4-5 |
| SDI | HD 10-bit channel width | - | 2-3 | 1 | - | 1 | 4-5 |
| | HD, 3G 20-bit channel width | - | 2-3 | 1 | - | 0.5 | 4-5 |
| BASIC Single Width | 8-bit/10-bit channel width | - | 2-3 | 1 | - | 1 | 4-5 |
| | 16-bit/20-bit channel width | - | 2-3 | 1 | - | 0.5 | 4-5 |
| BASIC Double Width | 16-bit/20-bit channel width | - | 2-3 | 1 | - | 1 | 4-5 |
| | 32-bit/40-bit channel width | - | 2-3 | 1 | - | 0.5 | 4-5 |
| | Parallel Loopback/ BIST | - | 2-3 | 1 | - | 1 | 4-5 |

Notes to Table 4–21:

- (1) The latency numbers are with respect to the PLD-transceiver interface clock cycles.
- (2) The total latency number is rounded off in the Sum column.
- (3) For CPRI 614 Mbps and 1.228 Gbps data rates, the Quartus II software customizes the PLD-transceiver interface clocking to achieve zero clock cycle uncertainty in the transmitter phase compensation FIFO latency. For more details, refer to the *CPRI Mode* section in the *Stratix II GX Transceiver Architecture Overview* chapter in volume 2 of the *Stratix II GX Device Handbook*.

Table 4-22. PCS Latency (Part 1 of 3) Note (1)

| Functional Mode | Configuration | Receiver PCS Latency | | | | | | | | | Sum (2) |
|---------------------|--|----------------------|-------------|---------------------|----------------|------------------------|--------------------|------------|--------------------------|---------------|------------|
| | | Word Aligner | Deskew FIFO | Rate Matcher (3) | 8B/10B Decoder | Receiver State Machine | Byte De-serializer | Byte Order | Receiver Phase Comp FIFO | Receiver PIPE | |
| XAUI | | 2-2.5 | 2-2.5 | 5.5-6.5 | 0.5 | 1 | 1 | 1 | 1-2 | - | 14-17 |
| PIPE | x1, x4, x8 8-bit channel width | 4-5 | - | 11-13 | 1 | - | 1 | 1 | 2-3 | 1 | 21-25 |
| | x1, x4, x8 16-bit channel width | 2-2.5 | - | 5.5-6.5 | 0.5 | - | 1 | 1 | 2-3 | 1 | 13-16 |
| GIGE | | 4-5 | - | 11-13 | 1 | - | 1 | 1 | 1-2 | - | 19-23 |
| SONET/ SDH | OC-12 | 6-7 | - | - | 1 | - | 1 | 1 | 1-2 | - | 10-12 |
| | OC-48 | 3-3.5 | - | - | 0.5 | - | 1 | 1-2 | 1-2 | - | 7-9 |
| | OC-96 | 2-2.5 | - | - | 0.5 | - | 1 | 1 | 1-2 | - | 6-7 |
| (OIF) CEI PHY | | 2.5 | - | - | 0.5 | - | 1 | 1 | 1-2 | - | 6-7 |
| CPRI (4) | 614 Mbps, 1.228 Gbps | 4-5 | - | - | 1 | - | 1 | 1 | 1 | - | 8-9 |
| | 2.456 Gbps | 4-5 | - | - | 1 | - | 1 | 1 | 1-2 | - | 8-10 |
| Serial RapidIO | 1.25 Gbps, 2.5 Gbps, 3.125 Gbps | 2-2.5 | - | - | 0.5 | - | 1 | 1 | 1-2 | - | 6-7 |
| SDI | HD 10-bit channel width | 5 | - | - | 1 | - | 1 | 1 | 1-2 | - | 9-10 |
| | HD, 3G 20-bit channel width | 2.5 | - | - | 0.5 | - | 1 | 1 | 1-2 | - | 6-7 |

Table 4–22. PCS Latency (Part 2 of 3) Note (1)

| Functional Mode | Configuration | Receiver PCS Latency | | | | | | | | | |
|--------------------|---|----------------------|-------------|------------------|----------------|------------------------|--------------------|------------|--------------------------|---------------|---------|
| | | Word Aligner | Deskew FIFO | Rate Matcher (3) | 8B/10B Decoder | Receiver State Machine | Byte De-serializer | Byte Order | Receiver Phase Comp FIFO | Receiver PIPE | Sum (2) |
| BASIC Single Width | 8/10-bit channel width; with Rate Matcher | 4-5 | - | 11-13 | 1 | - | 1 | 1 | 1-2 | 1 | 19-23 |
| | 8/10-bit channel width; without Rate Matcher | 4-5 | - | - | 1 | - | 1 | 1 | 1-2 | - | 8-10 |
| | 16/20-bit channel width; with Rate Matcher | 2-2.5 | - | 5.5-6.5 | 0.5 | - | 1 | 1 | 1-2 | - | 11-14 |
| | 16/20-bit channel width; without Rate Matcher | 2-2.5 | - | - | 0.5 | - | 1 | 1 | 1-2 | - | 6-7 |

Table 4–22. PCS Latency (Part 3 of 3) Note (1)

| Functional Mode | Configuration | Receiver PCS Latency | | | | | | | | | |
|--------------------|---|----------------------|-------------|------------------|----------------|------------------------|--------------------|------------|--------------------------|---------------|---------|
| | | Word Aligner | Deskew FIFO | Rate Matcher (3) | 8B/10B Decoder | Receiver State Machine | Byte De-serializer | Byte Order | Receiver Phase Comp FIFO | Receiver PIPE | Sum (2) |
| BASIC Double Width | 16/20-bit channel width; with Rate Matcher | 4-5 | - | 11-13 | 1 | - | 1 | 1 | 1-2 | - | 19-23 |
| | 16/20-bit channel width; without Rate Matcher | 4-5 | - | - | 1 | - | 1 | 1 | 1-2 | - | 8-10 |
| | 32/40-bit channel width; with Rate Matcher | 2-2.5 | - | 5.5-6.5 | 0.5 | - | 1 | 1 | 1-2 | - | 11-14 |
| | 32/40-bit channel width; without Rate Matcher | 2-2.5 | - | - | 0.5 | - | 1 | 1-3 | 1-2 | - | 6-9 |

Notes to Table 4–21:

- (1) The latency numbers are with respect to the PLD-transceiver interface clock cycles.
- (2) The total latency number is rounded off in the Sum column.
- (3) The rate matcher latency shown is the steady state latency. Actual latency may vary depending on the skip ordered set gap allowed by the protocol, actual PPM difference between the reference clocks, and so forth.
- (4) For CPRI 614 Mbps and 1.228 Gbps data rates, the Quartus II software customizes the PLD-transceiver interface clocking to achieve zero clock cycle uncertainty in the receiver phase compensation FIFO latency. For more details, refer to the CPRI Mode section in the *Stratix II GX Transceiver Architecture Overview* chapter in volume 2 of the *Stratix II GX Device Handbook*

DC Electrical Characteristics

Table 4–23 shows the Stratix II GX device family DC electrical characteristics.

| <i>Table 4–23. Stratix II GX Device DC Operating Conditions (Part 1 of 2) Note (1)</i> | | | | | | | |
|--|--------------------------------------|---|-----------|---------|---------|---------|---------|
| Symbol | Parameter | Conditions | Device | Minimum | Typical | Maximum | Unit |
| I_I | Input pin leakage current | $V_I = V_{CCIOmax}$ to 0 V (2) | All | –10 | | 10 | μ A |
| I_{OZ} | Tri-stated I/O pin leakage current | $V_O = V_{CCIOmax}$ to 0 V (2) | All | –10 | | 10 | μ A |
| I_{CCINT0} | V_{CCINT} supply current (standby) | $V_I =$ ground, no load, no toggling inputs $T_J = 25\text{ }^\circ\text{C}$ | EP2SGX30 | | 0.30 | (3) | A |
| | | | EP2SGX60 | | 0.50 | (3) | A |
| | | | EP2SGX90 | | 0.62 | (3) | A |
| | | | EP2SGX130 | | 0.82 | (3) | A |
| I_{CCPD0} | V_{CCPD} supply current (standby) | $V_I =$ ground, no load, no toggling inputs $T_J = 25\text{ }^\circ\text{C}$, $V_{CCPD} = 3.3\text{V}$ | EP2SGX30 | | 2.7 | (3) | mA |
| | | | EP2SGX60 | | 3.6 | (3) | mA |
| | | | EP2SGX90 | | 4.3 | (3) | mA |
| | | | EP2SGX130 | | 5.4 | (3) | mA |
| I_{CCIO0} | V_{CCIO} supply current (standby) | $V_I =$ ground, no load, no toggling inputs $T_J = 25\text{ }^\circ\text{C}$ | EP2SGX30 | | 4.0 | (3) | mA |
| | | | EP2SGX60 | | 4.0 | (3) | mA |
| | | | EP2SGX90 | | 4.0 | (3) | mA |
| | | | EP2SGX130 | | 4.0 | (3) | mA |

Table 4–23. Stratix II GX Device DC Operating Conditions (Part 2 of 2) *Note (1)*

| Symbol | Parameter | Conditions | Device | Minimum | Typical | Maximum | Unit |
|--------------------------|--|---|--------|---------|---------|---------|------|
| R _{CONF} (4) | Value of I/O pin pull-up resistor before and during configuration | V _i = 0, V _{CCIO} = 3.3 V | | 10 | 25 | 50 | KOhm |
| | | V _i = 0, V _{CCIO} = 2.5 V | | 15 | 35 | 70 | KOhm |
| | | V _i = 0, V _{CCIO} = 1.8 V | | 30 | 50 | 100 | KOhm |
| | | V _i = 0, V _{CCIO} = 1.5 V | | 40 | 75 | 150 | KOhm |
| | | V _i = 0, V _{CCIO} = 1.2 V | | 50 | 90 | 170 | KOhm |
| | Recommended value of I/O pin external pull-down resistor before and during configuration | | | | 1 | 2 | KOhm |

Notes to Table 4–23:

- (1) Typical values are for T_A = 25 °C, V_{CCINT} = 1.2 V, and V_{CCIO} = 1.5 V, 1.8 V, 2.5 V, and 3.3 V.
- (2) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).
- (3) Maximum values depend on the actual T_J and design utilization. See *PowerPlay Early Power Estimator (EPE) and Power Analyzer* or the *Quartus II PowerPlay Power Analyzer and Optimization Technology* (available at www.altera.com) for maximum values. See the section “Power Consumption” on page 4–59 for more information.
- (4) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO}.

I/O Standard Specifications

Tables 4–24 through 4–47 show the Stratix II GX device family I/O standard specifications.

Table 4–24. LVTTTL Specifications (Part 1 of 2)

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|-----------------------|---------------------------|-----------------------------|---------|---------|------|
| V _{CCIO} (1) | Output supply voltage | | 3.135 | 3.465 | V |
| V _{IH} | High-level input voltage | | 1.7 | 4.0 | V |
| V _{IL} | Low-level input voltage | | –0.3 | 0.8 | V |
| V _{OH} | High-level output voltage | I _{OH} = –4 mA (2) | 2.4 | | V |

Table 4–24. LVTTTL Specifications (Part 2 of 2)

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|----------|--------------------------|-----------------------------|---------|---------|------|
| V_{OL} | Low-level output voltage | $I_{OL} = 4 \text{ mA}$ (2) | | 0.45 | V |

Notes to Table 4–24:

- (1) Stratix II GX devices comply to the narrow range for the supply voltage as specified in the EIA/JEDEC Standard, JESD8-B.
- (2) This specification is supported across all the programmable drive strength settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–25. LVCMOS Specifications Note (1)

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|----------------|---------------------------|--|------------------|---------|------|
| V_{CCIO} (1) | Output supply voltage | | 3.135 | 3.465 | V |
| V_{IH} | High-level input voltage | | 1.7 | 4.0 | V |
| V_{IL} | Low-level input voltage | | –0.3 | 0.8 | V |
| V_{OH} | High-level output voltage | $V_{CCIO} = 3.0, I_{OH} = -0.1 \text{ mA}$ (2) | $V_{CCIO} - 0.2$ | | V |
| V_{OL} | Low-level output voltage | $V_{CCIO} = 3.0, I_{OL} = 0.1 \text{ mA}$ (2) | | 0.2 | V |

Notes to Table 4–25:

- (1) Stratix II GX devices comply to the narrow range for the supply voltage as specified in the EIA/JEDEC Standard, JESD8-B.
- (2) This specification is supported across all the programmable drive strength available for this I/O standard as shown in *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–26. 2.5-V I/O Specifications

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|----------------|---------------------------|------------------------------|---------|---------|------|
| V_{CCIO} (1) | Output supply voltage | | 2.375 | 2.625 | V |
| V_{IH} | High-level input voltage | | 1.7 | 4.0 | V |
| V_{IL} | Low-level input voltage | | –0.3 | 0.7 | V |
| V_{OH} | High-level output voltage | $I_{OH} = -1 \text{ mA}$ (2) | 2.0 | | V |
| V_{OL} | Low-level output voltage | $I_{OL} = 1 \text{ mA}$ (2) | | 0.4 | V |

Notes to Table 4–26:

- (1) The Stratix II GX device V_{CCIO} voltage level support of 2.5 to 5% is narrower than defined in the Normal Range of the EIA/JEDEC standard.
- (2) This specification is supported across all the programmable drive settings available for this I/O standard as shown in *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–27. 1.8-V I/O Specifications

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|----------------|---------------------------|------------------------------|------------------------|------------------------|------|
| V_{CCIO} (1) | Output supply voltage | | 1.71 | 1.89 | V |
| V_{IH} | High-level input voltage | | $0.65 \times V_{CCIO}$ | 2.25 | V |
| V_{IL} | Low-level input voltage | | -0.3 | $0.35 \times V_{CCIO}$ | V |
| V_{OH} | High-level output voltage | $I_{OH} = -2 \text{ mA}$ (2) | $V_{CCIO} - 0.45$ | | V |
| V_{OL} | Low-level output voltage | $I_{OL} = 2 \text{ mA}$ (2) | | 0.45 | V |

Notes to Table 4–27:

- (1) The Stratix II GX device V_{CCIO} voltage level support of 1.8 to 5% is narrower than defined in the Normal Range of the EIA/JEDEC standard.
- (2) This specification is supported across all the programmable drive settings available for this I/O standard as shown in *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–28. 1.5-V I/O Specifications

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|----------------|---------------------------|------------------------------|-----------------|------------------|------|
| V_{CCIO} (1) | Output supply voltage | | 1.425 | 1.575 | V |
| V_{IH} | High-level input voltage | | $0.65 V_{CCIO}$ | $V_{CCIO} + 0.3$ | V |
| V_{IL} | Low-level input voltage | | -0.3 | $0.35 V_{CCIO}$ | V |
| V_{OH} | High-level output voltage | $I_{OH} = -2 \text{ mA}$ (2) | $0.75 V_{CCIO}$ | | V |
| V_{OL} | Low-level output voltage | $I_{OL} = 2 \text{ mA}$ (2) | | $0.25 V_{CCIO}$ | V |

Notes to Table 4–28:

- (1) The Stratix II GX device V_{CCIO} voltage level support of 1.5 to 5% is narrower than defined in the Normal Range of the EIA/JEDEC standard.
- (2) This specification is supported across all the programmable drive settings available for this I/O standard as shown in *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Figures 4-6 and 4-7 show receiver input and transmitter output waveforms, respectively, for all differential I/O standards (LVDS and LVPECL).

Figure 4-6. Receiver Input Waveforms for Differential I/O Standards

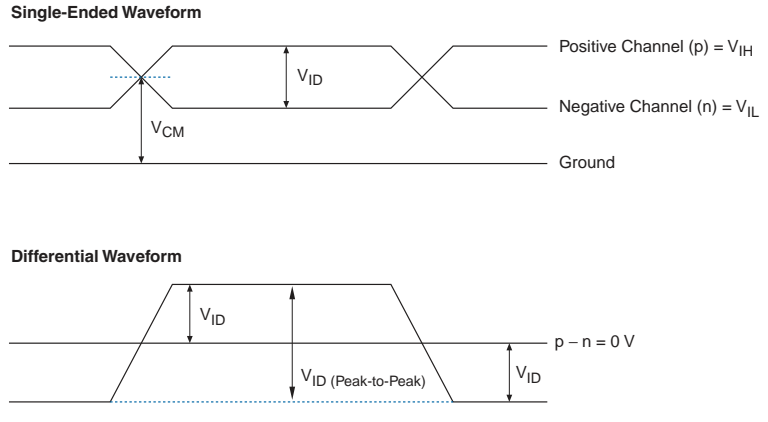


Figure 4-7. Transmitter Output Waveforms for Differential I/O Standards

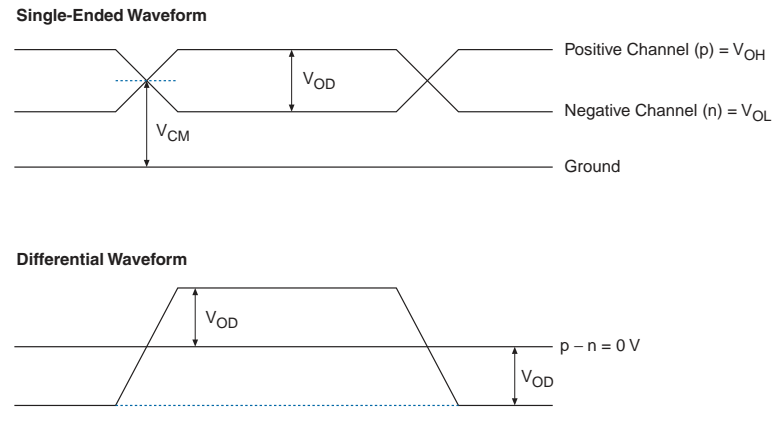


Table 4–29. 2.5-V LVDS I/O Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|------------|---|--------------------|---------|---------|---------|----------|
| V_{CCIO} | I/O supply voltage for left and right I/O banks (1, 2, 5, and 6) | | 2.375 | 2.5 | 2.625 | V |
| V_{ID} | Input differential voltage swing (single-ended) | | 100 | 350 | 900 | mV |
| V_{ICM} | Input common mode voltage | | 200 | 1,250 | 1,800 | mV |
| V_{OD} | Output differential voltage (single-ended) | $R_L = 100 \Omega$ | 250 | | 450 | mV |
| V_{OCM} | Output common mode voltage | $R_L = 100 \Omega$ | 1.125 | | 1.375 | V |
| R_L | Receiver differential input discrete resistor (external to Stratix II GX devices) | | 90 | 100 | 110 | Ω |

Table 4–30. 3.3-V LVDS I/O Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|----------------|---|--------------------|---------|---------|---------|----------|
| $V_{CCIO} (1)$ | I/O supply voltage for top and bottom PLL banks (9, 10, 11, and 12) | | 3.135 | 3.3 | 3.465 | V |
| V_{ID} | Input differential voltage swing (single-ended) | | 100 | 350 | 900 | mV |
| V_{ICM} | Input common mode voltage | | 200 | 1,250 | 1,800 | mV |
| V_{OD} | Output differential voltage (single-ended) | $R_L = 100 \Omega$ | 250 | | 710 | mV |
| V_{OCM} | Output common mode voltage | $R_L = 100 \Omega$ | 840 | | 1,570 | mV |
| R_L | Receiver differential input discrete resistor (external to Stratix II GX devices) | | 90 | 100 | 110 | Ω |

Note to Table 4–30:

- (1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT} , not V_{CCIO} . The PLL clock output/feedback differential buffers are powered by VCC_PLL_OUT . For differential clock output/feedback operation, connect VCC_PLL_OUT to 3.3 V.

| Table 4–31. PCML Specifications <i>Note (1)</i> | | |
|--|---|---|
| Symbol | Parameter | References |
| Reference Clock | | |
| 3.3-V PCML 1.5-V PCML 1.2-V PCML | Reference clock supported PCML standards | |
| V_{ID} | Peak-to-peak differential input voltage | The specifications are located in the Reference Clock section of Table 4–6 on page 4–4 . |
| V_{ICM} | Input common mode voltage | The specifications listed in Table 4–6 are applicable to PCML input standards. |
| R | On-chip termination resistors | |
| Receiver | | |
| 3.3-V PCML 1.5-V PCML 1.2-V PCML | Receiver supported PCML standards | |
| V_{ID} | Peak-to-peak differential input voltage | The specifications are located in the Receiver section of Table 4–6 on page 4–4 . |
| V_{ICM} | Input common mode voltage | The specifications listed in Table 4–6 are applicable to PCML input standards. |
| R | On-chip termination resistors | |
| Transmitter | | |
| 1.5-V PCML 1.2-V PCML | Transmitter supported PCML standards | |
| V_{CCH} | Output buffer supply voltage | The specifications are located in Table 4–5 on page 4–4 . |
| V_{OD} | Peak-to-peak differential output voltage | The specifications are located in Tables 4–7, 4–8, 4–9, 4–10, 4–11, and 4–12 . The specifications listed in these tables are applicable to PCML output standards. |
| V_{OCM} | Output common mode voltage | The specifications are located in the Transmitter section of Table 4–6 on page 4–4 . |
| R | On-chip termination resistors | The specifications listed in Table 4–6 are applicable to PCML output standards. |

Note to Table 4–31:

- (1) Stratix II GX devices support PCML input and output on GXB banks 13, 14, 15, 16, and 17. This table references Stratix II GX PCML specifications that are located in other sections of the *Stratix II GX Device Handbook*.

Table 4–32. LVPECL Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|----------------|---|--------------------|---------|---------|---------|----------|
| V_{CCIO} (1) | I/O supply voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{ID} | Input differential voltage swing (single-ended) | | 300 | 600 | 1,000 | mV |
| V_{ICM} | Input common mode voltage | | 1.0 | | 2.5 | V |
| V_{OD} | Output differential voltage (single-ended) | $R_L = 100 \Omega$ | 525 | | 970 | mV |
| V_{OCM} | Output common mode voltage | $R_L = 100 \Omega$ | 1,650 | | 2,250 | mV |
| R_L | Receiver differential input resistor | | 90 | 100 | 110 | Ω |

Note to Table 4–32:

- (1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT} , not V_{CCIO} . The PLL clock output/feedback differential buffers are powered by VCC_PLL_OUT . For differential clock output/feedback operation, connect VCC_PLL_OUT to 3.3 V.

Table 4–33. 3.3-V PCI Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|------------|---------------------------|-------------------------|----------------|---------|------------------|------|
| V_{CCIO} | Output supply voltage | | 3.0 | 3.3 | 3.6 | V |
| V_{IH} | High-level input voltage | | $0.5 V_{CCIO}$ | | $V_{CCIO} + 0.5$ | V |
| V_{IL} | Low-level input voltage | | -0.3 | | $0.3 V_{CCIO}$ | V |
| V_{OH} | High-level output voltage | $I_{OUT} = -500 \mu A$ | $0.9 V_{CCIO}$ | | | V |
| V_{OL} | Low-level output voltage | $I_{OUT} = 1,500 \mu A$ | | | $0.1 V_{CCIO}$ | V |

Table 4–34. PCI-X Mode 1 Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|------------|---------------------------|-------------------------|----------------|---------|------------------|------|
| V_{CCIO} | Output supply voltage | | 3.0 | | 3.6 | V |
| V_{IH} | High-level input voltage | | $0.5 V_{CCIO}$ | | $V_{CCIO} + 0.5$ | V |
| V_{IL} | Low-level input voltage | | -0.3 | | $0.35 V_{CCIO}$ | V |
| V_{IPU} | Input pull-up voltage | | $0.7 V_{CCIO}$ | | | V |
| V_{OH} | High-level output voltage | $I_{OUT} = -500 \mu A$ | $0.9 V_{CCIO}$ | | | V |
| V_{OL} | Low-level output voltage | $I_{OUT} = 1,500 \mu A$ | | | $0.1 V_{CCIO}$ | V |

Table 4–35. SSTL-18 Class I Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---------------|-----------------------------|--------------------------------|-------------------|-----------|-------------------|------|
| V_{CCIO} | Output supply voltage | | 1.71 | 1.8 | 1.89 | V |
| V_{REF} | Reference voltage | | 0.855 | 0.9 | 0.945 | V |
| V_{TT} | Termination voltage | | $V_{REF} - 0.04$ | V_{REF} | $V_{REF} + 0.04$ | V |
| $V_{IH} (DC)$ | High-level DC input voltage | | $V_{REF} + 0.125$ | | | V |
| $V_{IL} (DC)$ | Low-level DC input voltage | | | | $V_{REF} - 0.125$ | V |
| $V_{IH} (AC)$ | High-level AC input voltage | | $V_{REF} + 0.25$ | | | V |
| $V_{IL} (AC)$ | Low-level AC input voltage | | | | $V_{REF} - 0.25$ | V |
| V_{OH} | High-level output voltage | $I_{OH} = -6.7 \text{ mA}$ (1) | $V_{TT} + 0.475$ | | | V |
| V_{OL} | Low-level output voltage | $I_{OL} = 6.7 \text{ mA}$ (1) | | | $V_{TT} - 0.475$ | V |

Note to Table 4–35:

- (1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–36. SSTL-18 Class II Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---------------|-----------------------------|---------------------------------|-------------------|-----------|-------------------|------|
| V_{CCIO} | Output supply voltage | | 1.71 | 1.8 | 1.89 | V |
| V_{REF} | Reference voltage | | 0.855 | 0.9 | 0.945 | V |
| V_{TT} | Termination voltage | | $V_{REF} - 0.04$ | V_{REF} | $V_{REF} + 0.04$ | V |
| $V_{IH} (DC)$ | High-level DC input voltage | | $V_{REF} + 0.125$ | | | V |
| $V_{IL} (DC)$ | Low-level DC input voltage | | | | $V_{REF} - 0.125$ | V |
| $V_{IH} (AC)$ | High-level AC input voltage | | $V_{REF} + 0.25$ | | | V |
| $V_{IL} (AC)$ | Low-level AC input voltage | | | | $V_{REF} - 0.25$ | V |
| V_{OH} | High-level output voltage | $I_{OH} = -13.4 \text{ mA}$ (1) | $V_{CCIO} - 0.28$ | | | V |
| V_{OL} | Low-level output voltage | $I_{OL} = 13.4 \text{ mA}$ (1) | | | 0.28 | V |

Note to Table 4–36:

- (1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–37. SSTL-18 Class I and II Differential Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|------------------|---|------------|------------------------|----------------|------------------------|------|
| V_{CCIO} | Output supply voltage | | 1.71 | 1.8 | 1.89 | V |
| V_{SWING} (DC) | DC differential input voltage | | 0.25 | | | V |
| V_X (AC) | AC differential input cross point voltage | | $(V_{CCIO}/2) - 0.175$ | | $(V_{CCIO}/2) + 0.175$ | V |
| V_{SWING} (AC) | AC differential input voltage | | 0.5 | | | V |
| V_{ISO} | Input clock signal offset voltage | | | $0.5 V_{CCIO}$ | | V |
| ΔV_{ISO} | Input clock signal offset voltage variation | | | 200 | | mV |
| V_{OX} (AC) | AC differential cross point voltage | | $(V_{CCIO}/2) - 0.125$ | | $(V_{CCIO}/2) + 0.125$ | V |

Table 4–38. SSTL-2 Class I Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---------------|-----------------------------|--------------------------------|------------------|-----------|------------------|------|
| V_{CCIO} | Output supply voltage | | 2.375 | 2.5 | 2.625 | V |
| V_{TT} | Termination voltage | | $V_{REF} - 0.04$ | V_{REF} | $V_{REF} + 0.04$ | V |
| V_{REF} | Reference voltage | | 1.188 | 1.25 | 1.313 | V |
| V_{IH} (DC) | High-level DC input voltage | | $V_{REF} + 0.18$ | | 3.0 | V |
| V_{IL} (DC) | Low-level DC input voltage | | -0.3 | | $V_{REF} - 0.18$ | V |
| V_{IH} (AC) | High-level AC input voltage | | $V_{REF} + 0.35$ | | | V |
| V_{IL} (AC) | Low-level AC input voltage | | | | $V_{REF} - 0.35$ | V |
| V_{OH} | High-level output voltage | $I_{OH} = -8.1 \text{ mA}$ (1) | $V_{TT} + 0.57$ | | | V |
| V_{OL} | Low-level output voltage | $I_{OL} = 8.1 \text{ mA}$ (1) | | | $V_{TT} - 0.57$ | V |

Note to Table 4–38:

- (1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–39. SSTL-2 Class II Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|------------|-----------------------|------------|------------------|-----------|------------------|------|
| V_{CCIO} | Output supply voltage | | 2.375 | 2.5 | 2.625 | V |
| V_{TT} | Termination voltage | | $V_{REF} - 0.04$ | V_{REF} | $V_{REF} + 0.04$ | V |
| V_{REF} | Reference voltage | | 1.188 | 1.25 | 1.313 | V |

Table 4–39. SSTL-2 Class II Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---------------|-----------------------------|---------------------------------|------------------|---------|------------------|------|
| V_{IH} (DC) | High-level DC input voltage | | $V_{REF} + 0.18$ | | $V_{CCIO} + 0.3$ | V |
| V_{IL} (DC) | Low-level DC input voltage | | -0.3 | | $V_{REF} - 0.18$ | V |
| V_{IH} (AC) | High-level AC input voltage | | $V_{REF} + 0.35$ | | | V |
| V_{IL} (AC) | Low-level AC input voltage | | | | $V_{REF} - 0.35$ | V |
| V_{OH} | High-level output voltage | $I_{OH} = -16.4 \text{ mA}$ (1) | $V_{TT} + 0.76$ | | | V |
| V_{OL} | Low-level output voltage | $I_{OL} = 16.4 \text{ mA}$ (1) | | | $V_{TT} - 0.76$ | V |

Note to Table 4–39:

- (1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–40. SSTL-2 Class I and II Differential Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|------------------|---|------------|----------------------|----------------|----------------------|------|
| V_{CCIO} | Output supply voltage | | 2.375 | 2.5 | 2.625 | V |
| V_{SWING} (DC) | DC differential input voltage | | 0.36 | | | V |
| V_X (AC) | AC differential input cross point voltage | | $(V_{CCIO}/2) - 0.2$ | | $(V_{CCIO}/2) + 0.2$ | V |
| V_{SWING} (AC) | AC differential input voltage | | 0.7 | | | V |
| V_{ISO} | Input clock signal offset voltage | | | $0.5 V_{CCIO}$ | | V |
| ΔV_{ISO} | Input clock signal offset voltage variation | | | 200 | | mV |
| V_{OX} (AC) | AC differential output cross point voltage | | $(V_{CCIO}/2) - 0.2$ | | $(V_{CCIO}/2) + 0.2$ | V |

Table 4–41. 1.2-V HSTL Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---------------|-----------------------------|------------|------------------|----------------|-------------------|------|
| V_{CCIO} | Output supply voltage | | 1.14 | 1.2 | 1.26 | V |
| V_{REF} | Reference voltage | | $0.48 V_{CCIO}$ | $0.5 V_{CCIO}$ | $0.52 V_{CCIO}$ | V |
| V_{IH} (DC) | High-level DC input voltage | | $V_{REF} + 0.08$ | | $V_{CCIO} + 0.15$ | V |
| V_{IL} (DC) | Low-level DC input voltage | | -0.15 | | $V_{REF} - 0.08$ | V |
| V_{IH} (AC) | High-level AC input voltage | | $V_{REF} + 0.15$ | | $V_{CCIO} + 0.24$ | V |
| V_{IL} (AC) | Low-level AC input voltage | | -0.24 | | $V_{REF} - 0.15$ | V |

Table 4–41. 1.2-V HSTL Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|-----------------|---------------------------|-------------------------|-------------------------|---------|--------------------------|------|
| V _{OH} | High-level output voltage | I _{OH} = 8 mA | V _{REF} + 0.15 | | V _{CCIO} + 0.15 | V |
| V _{OL} | Low-level output voltage | I _{OH} = –8 mA | –0.15 | | V _{REF} – 0.15 | V |

Table 4–42. 1.5-V HSTL Class I Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|----------------------|-----------------------------|-----------------------------|-------------------------|---------|------------------------|------|
| V _{CCIO} | Output supply voltage | | 1.425 | 1.5 | 1.575 | V |
| V _{REF} | Input reference voltage | | 0.713 | 0.75 | 0.788 | V |
| V _{TT} | Termination voltage | | 0.713 | 0.75 | 0.788 | V |
| V _{IH} (DC) | DC high-level input voltage | | V _{REF} + 0.1 | | | V |
| V _{IL} (DC) | DC low-level input voltage | | –0.3 | | V _{REF} – 0.1 | V |
| V _{IH} (AC) | AC high-level input voltage | | V _{REF} + 0.2 | | | V |
| V _{IL} (AC) | AC low-level input voltage | | | | V _{REF} – 0.2 | V |
| V _{OH} | High-level output voltage | I _{OH} = 8 mA (1) | V _{CCIO} – 0.4 | | | V |
| V _{OL} | Low-level output voltage | I _{OH} = –8 mA (1) | | | 0.4 | V |

Note to Table 4–42:

- (1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–43. 1.5-V HSTL Class II Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|----------------------|-----------------------------|------------------------------|-------------------------|---------|------------------------|------|
| V _{CCIO} | Output supply voltage | | 1.425 | 1.50 | 1.575 | V |
| V _{REF} | Input reference voltage | | 0.713 | 0.75 | 0.788 | V |
| V _{TT} | Termination voltage | | 0.713 | 0.75 | 0.788 | V |
| V _{IH} (DC) | DC high-level input voltage | | V _{REF} + 0.1 | | | V |
| V _{IL} (DC) | DC low-level input voltage | | –0.3 | | V _{REF} – 0.1 | V |
| V _{IH} (AC) | AC high-level input voltage | | V _{REF} + 0.2 | | | V |
| V _{IL} (AC) | AC low-level input voltage | | | | V _{REF} – 0.2 | V |
| V _{OH} | High-level output voltage | I _{OH} = 16 mA (1) | V _{CCIO} – 0.4 | | | V |
| V _{OL} | Low-level output voltage | I _{OH} = –16 mA (1) | | | 0.4 | V |

Note to Table 4–43:

- (1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–44. 1.5-V HSTL Class I and II Differential Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|----------------|-------------------------------------|------------|---------|---------|---------|------|
| V_{CCIO} | I/O supply voltage | | 1.425 | 1.5 | 1.575 | V |
| V_{DIF} (DC) | DC input differential voltage | | 0.2 | | | V |
| V_{CM} (DC) | DC common mode input voltage | | 0.68 | | 0.9 | V |
| V_{DIF} (AC) | AC differential input voltage | | 0.4 | | | V |
| V_{OX} (AC) | AC differential cross point voltage | | 0.68 | | 0.9 | V |

Table 4–45. 1.8-V HSTL Class I Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---------------|-----------------------------|------------------------------|------------------|---------|-----------------|------|
| V_{CCIO} | Output supply voltage | | 1.71 | 1.80 | 1.89 | V |
| V_{REF} | Input reference voltage | | 0.85 | 0.90 | 0.95 | V |
| V_{TT} | Termination voltage | | 0.85 | 0.90 | 0.95 | V |
| V_{IH} (DC) | DC high-level input voltage | | $V_{REF} + 0.1$ | | | V |
| V_{IL} (DC) | DC low-level input voltage | | -0.3 | | $V_{REF} - 0.1$ | V |
| V_{IH} (AC) | AC high-level input voltage | | $V_{REF} + 0.2$ | | | V |
| V_{IL} (AC) | AC low-level input voltage | | | | $V_{REF} - 0.2$ | V |
| V_{OH} | High-level output voltage | $I_{OH} = 8 \text{ mA}$ (1) | $V_{CCIO} - 0.4$ | | | V |
| V_{OL} | Low-level output voltage | $I_{OH} = -8 \text{ mA}$ (1) | | | 0.4 | V |

Note to Table 4–45:

- (1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–46. 1.8-V HSTL Class II Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---------------|-----------------------------|-------------------------------|------------------|---------|-----------------|------|
| V_{CCIO} | Output supply voltage | | 1.71 | 1.80 | 1.89 | V |
| V_{REF} | Input reference voltage | | 0.85 | 0.90 | 0.95 | V |
| V_{TT} | Termination voltage | | 0.85 | 0.90 | 0.95 | V |
| V_{IH} (DC) | DC high-level input voltage | | $V_{REF} + 0.1$ | | | V |
| V_{IL} (DC) | DC low-level input voltage | | -0.3 | | $V_{REF} - 0.1$ | V |
| V_{IH} (AC) | AC high-level input voltage | | $V_{REF} + 0.2$ | | | V |
| V_{IL} (AC) | AC low-level input voltage | | | | $V_{REF} - 0.2$ | V |
| V_{OH} | High-level output voltage | $I_{OH} = 16 \text{ mA}$ (1) | $V_{CCIO} - 0.4$ | | | V |
| V_{OL} | Low-level output voltage | $I_{OH} = -16 \text{ mA}$ (1) | | | 0.4 | V |

Note to Table 4–46:

- (1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–47. 1.8-V HSTL Class I and II Differential Specifications

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|----------------|-------------------------------------|------------|---------|---------|---------|------|
| V_{CCIO} | I/O supply voltage | | 1.71 | 1.80 | 1.89 | V |
| V_{DIF} (DC) | DC input differential voltage | | 0.2 | | | V |
| V_{CM} (DC) | DC common mode input voltage | | 0.78 | | 1.12 | V |
| V_{DIF} (AC) | AC differential input voltage | | 0.4 | | | V |
| V_{OX} (AC) | AC differential cross point voltage | | 0.68 | | 0.9 | V |

Bus Hold Specifications

Table 4–48 shows the Stratix II GX device family bus hold specifications.

Table 4–48. Bus Hold Parameters

| Parameter | Conditions | V_{CCIO} Level | | | | | | | | | | Unit |
|-------------------------|--------------------------------|------------------|------|-------|------|-------|------|-------|------|-------|------|---------|
| | | 1.2 V | | 1.5 V | | 1.8 V | | 2.5 V | | 3.3 V | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Low sustaining current | $V_{IN} > V_{IL}$ (maximum) | 22.5 | | 25 | | 30 | | 50 | | 70 | | μA |
| High sustaining current | $V_{IN} < V_{IH}$ (minimum) | -22.5 | | -25 | | -30 | | -50 | | -70 | | μA |
| Low overdrive current | $0 V < V_{IN} < V_{CCIO}$ | | 120 | | 160 | | 200 | | 300 | | 500 | μA |
| High overdrive current | $0 V < V_{IN} < V_{CCIO}$ | | -120 | | -160 | | -200 | | -300 | | -500 | μA |
| Bus-hold trip point | | 0.45 | 0.95 | 0.5 | 1.0 | 0.68 | 1.07 | 0.7 | 1.7 | 0.8 | 2.0 | V |

On-Chip Termination Specifications

Tables 4–49 and 4–50 define the specification for internal termination resistance tolerance when using series or differential on-chip termination.

Table 4–49. On-Chip Termination Specification for Top and Bottom I/O Banks (Part 1 of 2) Notes (1), (2)

| Symbol | Description | Conditions | Resistance Tolerance | | |
|-------------------------------|--|------------------------|----------------------|----------------|------|
| | | | Commercial Max | Industrial Max | Unit |
| 25- Ω R_S 3.3/2.5 | Internal series termination with calibration (25- Ω setting) | $V_{CCIO} = 3.3/2.5 V$ | ± 5 | ± 10 | % |
| | Internal series termination without calibration (25- Ω setting) | $V_{CCIO} = 3.3/2.5 V$ | ± 30 | ± 30 | % |
| 50- Ω R_S 3.3/2.5 | Internal series termination with calibration (50- Ω setting) | $V_{CCIO} = 3.3/2.5 V$ | ± 5 | ± 10 | % |
| | Internal series termination without calibration (50- Ω setting) | $V_{CCIO} = 3.3/2.5 V$ | ± 30 | ± 30 | % |

Table 4–49. On-Chip Termination Specification for Top and Bottom I/O Banks (Part 2 of 2) Notes (1), (2)

| Symbol | Description | Conditions | Resistance Tolerance | | |
|----------------------------|--|---------------------------|----------------------|----------------|------|
| | | | Commercial Max | Industrial Max | Unit |
| 50-Ω R _T 2.5 | Internal parallel termination with calibration (50-Ω setting) | V _{CCIO} = 1.8 V | ±30 | ± 30 | % |
| 25-Ω R _S 1.8 | Internal series termination with calibration (25-Ω setting) | V _{CCIO} = 1.8 V | ±5 | ±10 | % |
| | Internal series termination without calibration (25-Ω setting) | V _{CCIO} = 1.8 V | ±30 | ±30 | % |
| 50-Ω R _S 1.8 | Internal series termination with calibration (50-Ω setting) | V _{CCIO} = 1.8 V | ±5 | ±10 | % |
| | Internal series termination without calibration (50-Ω setting) | V _{CCIO} = 1.8 V | ±30 | ±30 | % |
| 50-Ω R _T 1.8 | Internal parallel termination with calibration (50-Ω setting) | V _{CCIO} = 1.8 V | ±10 | ±15 | % |
| 50-Ω R _S 1.5 | Internal series termination with calibration (50-Ω setting) | V _{CCIO} = 1.5 V | ±8 | ±10 | % |
| | Internal series termination without calibration (50-Ω setting) | V _{CCIO} = 1.5 V | ±36 | ±36 | % |
| 50-Ω R _T 1.5 | Internal parallel termination with calibration (50-Ω setting) | V _{CCIO} = 1.5 V | ±10 | ±15 | % |
| 50-Ω R _S 1.2 | Internal series termination with calibration (50-Ω setting) | V _{CCIO} = 1.2 V | ±8 | ±10 | % |
| | Internal series termination without calibration (50-Ω setting) | V _{CCIO} = 1.2 V | ±50 | ±50 | % |
| 50-Ω R _T 1.2 | Internal parallel termination with calibration (50-Ω setting) | V _{CCIO} = 1.2 V | ±10 | ±15 | % |

Note for Table 4–49:

- (1) The resistance tolerance for calibrated SOCT is for the moment of calibration. If the temperature or voltage changes over time, the tolerance may also change.
- (2) On-chip parallel termination with calibration is only supported for input pins.

Table 4–50. Series and Differential On-Chip Termination Specification for Left I/O Banks *Note (1)*

| Symbol | Description | Conditions | Resistance Tolerance | | |
|------------------------------------|--|----------------------------------|----------------------|----------------|------|
| | | | Commercial Max | Industrial Max | Unit |
| 25-Ω R _S 3.3/2.5 | Internal series termination without calibration (25-Ω setting) | V _{CCIO} = 3.3/2.5V | ±30 | ±30 | % |
| 50-Ω R _S 3.3/2.5/1.8 | Internal series termination without calibration (50-Ω setting) | V _{CCIO} = 3.3/2.5/1.8V | ±30 | ±30 | % |
| 50-Ω R _S 1.5 | Internal series termination without calibration (50-Ω setting) | V _{CCIO} = 1.5V | ±36 | ±36 | % |
| R _D | Internal differential termination for LVDS (100-Ω setting) | V _{CCIO} = 2.5 V | ±20 | ±25 | % |

Note to Table 4–50:

- (1) On-chip parallel termination with calibration is only supported for input pins.

Pin Capacitance

Table 4–51 shows the Stratix II GX device family pin capacitance.

Table 4–51. Stratix II GX Device Capacitance *Note (1)*

| Symbol | Parameter | Typical | Unit |
|--------------------|--|---------|------|
| C _{IOTB} | Input capacitance on I/O pins in I/O banks 3, 4, 7, and 8. | 5.0 | pF |
| C _{IOL} | Input capacitance on I/O pins in I/O banks 1 and 2, including high-speed differential receiver and transmitter pins. | 6.1 | pF |
| C _{CLKTB} | Input capacitance on top/bottom clock input pins: CLK [4 . . 7] and CLK [12 . . 15]. | 6.0 | pF |
| C _{CLKL} | Input capacitance on left clock inputs: CLK0 and CLK2. | 6.1 | pF |
| C _{CLKL+} | Input capacitance on left clock inputs: CLK1 and CLK3. | 3.3 | pF |
| C _{OUTFB} | Input capacitance on dual-purpose clock output/feedback pins in PLL banks 11 and 12. | 6.7 | pF |

Note to Table 4–51:

- (1) Capacitance is sample-tested only. Capacitance is measured using time-domain reflections (TDR). Measurement accuracy is within ±0.5 pF.

Power Consumption

Altera offers two ways to calculate power for a design: the Excel-based PowerPlay early power estimator power calculator and the Quartus® II PowerPlay power analyzer feature.

The interactive Excel-based PowerPlay early power estimator is typically used prior to designing the FPGA in order to get an estimate of device power. The Quartus II PowerPlay power analyzer provides better quality estimates based on the specifics of the design after place-and-route is complete. The power analyzer can apply a combination of user-entered, simulation-derived and estimated signal activities which, combined with detailed circuit models, can yield very accurate power estimates.

In both cases, these calculations should only be used as an estimation of power, not as a specification.



For more information on PowerPlay tools, refer to the *PowerPlay Early Power Estimators (EPE) and Power Analyzer*, the *Quartus II PowerPlay Analysis and Optimization Technology*, and the *PowerPlay Power Analyzer* chapter in volume 3 of the *Quartus II Handbook*. The PowerPlay early power estimators are available on the Altera web site at www.altera.com.



See [Table 4–23 on page 42](#) for typical I_{CC} standby specifications.

Timing Model

The DirectDrive technology and MultiTrack interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Stratix II GX device densities and speed grades. This section describes and specifies the performance, internal, external, and PLL timing specifications.

All specifications are representative of worst-case supply voltage and junction temperature conditions.

Preliminary and Final Timing

Timing models can have either preliminary or final status. The Quartus II software issues an informational message during the design compilation if the timing models are preliminary. [Table 4–52](#) shows the status of the Stratix II GX device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

Table 4–52. Stratix II GX Device Timing Model Status

| Device | Preliminary | Final |
|-----------|-------------|-------|
| EP2SGX30 | | ✓ |
| EP2SGX60 | | ✓ |
| EP2SGX90 | | ✓ |
| EP2SGX130 | | ✓ |

I/O Timing Measurement Methodology

Different I/O standards require different baseline loading techniques for reporting timing delays. Altera characterizes timing delays with the required termination for each I/O standard and with 0 pF (except for PCI and PCI-X which use 10 pF) loading and the timing is specified up to the output pin of the FPGA device. The Quartus II software calculates the I/O timing for each I/O standard with a default baseline loading as specified by the I/O standards.

The following measurements are made during device characterization. Altera measures clock-to-output delays (t_{CO}) at worst-case process, minimum voltage, and maximum temperature (PVT) for default loading conditions shown in Table 4–53. Use the following equations to calculate clock pin to output pin timing for Stratix II GX devices.

$$t_{CO} \text{ from clock pin to I/O pin} = \text{delay from clock pad to I/O output register} + \text{IOE output register clock-to-output delay} + \text{delay from output register to output pin} + \text{I/O output delay}$$

$$t_{xz}/t_{zx} \text{ from clock pin to I/O pin} = \text{delay from clock pad to I/O output register} + \text{IOE output register clock-to-output delay} + \text{delay from output register to output pin} + \text{I/O output delay} + \text{output enable pin delay}$$

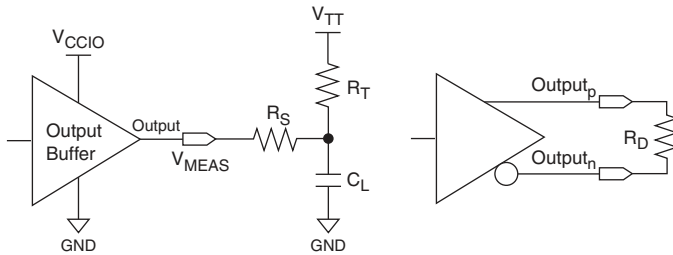
Simulation using IBIS models is required to determine the delays on the PCB traces in addition to the output pin delay timing reported by the Quartus II software and the timing model in the device handbook.

1. Simulate the output driver of choice into the generalized test setup, using values from Table 4–53.
2. Record the time to V_{MEAS} .

3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS} .
5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Standard Output Adder delays to yield the actual worst-case propagation delay (clock-to-output) of the PCB trace.

The Quartus II software reports the timing with the conditions shown in Table 4–53 using the above equation. Figure 4–8 shows the model of the circuit that is represented by the output timing of the Quartus II software.

Figure 4–8. Output Delay Timing Reporting Setup Modeled by Quartus II



Notes to Figure 4–8:

- (1) Output pin timing is reported at the output pin of the FPGA device. Additional delays for loading and board trace delay need to be accounted for with IBIS model simulations.
- (2) V_{CCPD} is 3.085 V unless otherwise specified.
- (3) V_{CCINT} is 1.12 V unless otherwise specified.

| I/O Standard | Loading and Termination | | | | | | Measurement Point |
|--------------|-------------------------|--------------------|--------------------|----------------|--------------|------------|-------------------|
| | R_S (Ω) | R_D (Ω) | R_T (Ω) | V_{CCIO} (V) | V_{TT} (V) | C_L (pF) | V_{MEAS} (V) |
| LVTTTL (4) | | | | 3.135 | | 0 | 1.5675 |
| LVC MOS (4) | | | | 3.135 | | 0 | 1.5675 |
| 2.5 V (4) | | | | 2.375 | | 0 | 1.1875 |
| 1.8 V (4) | | | | 1.710 | | 0 | 0.855 |
| 1.5 V (4) | | | | 1.425 | | 0 | 0.7125 |

Table 4–53. Output Timing Measurement Methodology for Output Pins (Part 2 of 2) Notes (1), (2), (3)

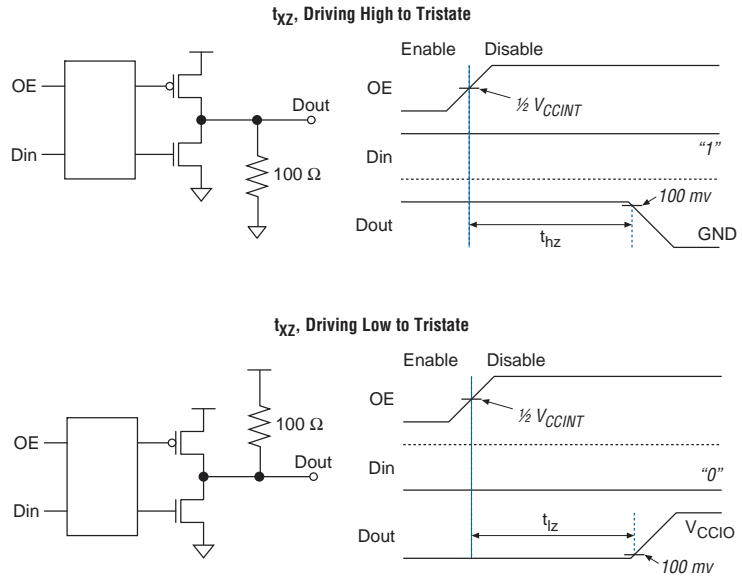
| I/O Standard | Loading and Termination | | | | | | Measurement Point |
|----------------------------------|-------------------------|--------------------|--------------------|----------------|--------------|------------|-------------------|
| | R_S (Ω) | R_D (Ω) | R_T (Ω) | V_{CCIO} (V) | V_{TT} (V) | C_L (pF) | V_{MEAS} (V) |
| PCI (5) | | | | 2.970 | | 10 | 1.485 |
| PCI-X (5) | | | | 2.970 | | 10 | 1.485 |
| SSTL-2 Class I | 25 | | 50 | 2.325 | 1.123 | 0 | 1.1625 |
| SSTL-2 Class II | 25 | | 25 | 2.325 | 1.123 | 0 | 1.1625 |
| SSTL-18 Class I | 25 | | 50 | 1.660 | 0.790 | 0 | 0.83 |
| SSTL-18 Class II | 25 | | 25 | 1.660 | 0.790 | 0 | 0.83 |
| 1.8-V HSTL Class I | | | 50 | 1.660 | 0.790 | 0 | 0.83 |
| 1.8-V HSTL Class II | | | 25 | 1.660 | 0.790 | 0 | 0.83 |
| 1.5-V HSTL Class I | | | 50 | 1.375 | 0.648 | 0 | 0.6875 |
| 1.5-V HSTL Class II | | | 25 | 1.375 | 0.648 | 0 | 0.6875 |
| 1.2-V HSTL with OCT | | | | 1.140 | | 0 | 0.570 |
| Differential SSTL-2 Class I | 25 | | 50 | 2.325 | 1.123 | 0 | 1.1625 |
| Differential SSTL-2 Class II | 25 | | 25 | 2.325 | 1.123 | 0 | 1.1625 |
| Differential SSTL-18 Class I | 50 | | 50 | 1.660 | 0.790 | 0 | 0.83 |
| Differential SSTL-18 Class II | 25 | | 25 | 1.660 | 0.790 | 0 | 0.83 |
| 1.5-V differential HSTL Class I | | | 50 | 1.375 | 0.648 | 0 | 0.6875 |
| 1.5-V differential HSTL Class II | | | 25 | 1.375 | 0.648 | 0 | 0.6875 |
| 1.8-V differential HSTL Class I | | | 50 | 1.660 | 0.790 | 0 | 0.83 |
| 1.8-V differential HSTL Class II | | | 25 | 1.660 | 0.790 | 0 | 0.83 |
| LVDS | | 100 | | 2.325 | | 0 | 1.1625 |
| LVPECL | | 100 | | 3.135 | | 0 | 1.5675 |

Notes to Table 4–53:

- (1) Input measurement point at internal node is $0.5 V_{CCINT}$.
- (2) Output measuring point for V_{MEAS} at buffer output is $0.5 V_{CCIO}$.
- (3) Input stimulus edge rate is 0 to V_{CC} in 0.2 ns (internal signal) from the driver preceding the I/O buffer.
- (4) Less than 50-mV ripple on V_{CCIO} and V_{CCPD} , $V_{CCINT} = 1.15$ V with less than 30-mV ripple.
- (5) $V_{CCPD} = 2.97$ V, less than 50-mV ripple on V_{CCIO} and V_{CCPD} , $V_{CCINT} = 1.15$ V.

Figures 4-9 and 4-10 show the measurement setup for output disable and output enable timing.

Figure 4-9. Measurement Setup for t_{xz} Note (1)



Note to Figure 4-9:

(1) V_{CCINT} is 1.12 V for this measurement.

Figure 4–10. Measurement Setup for t_{zx}

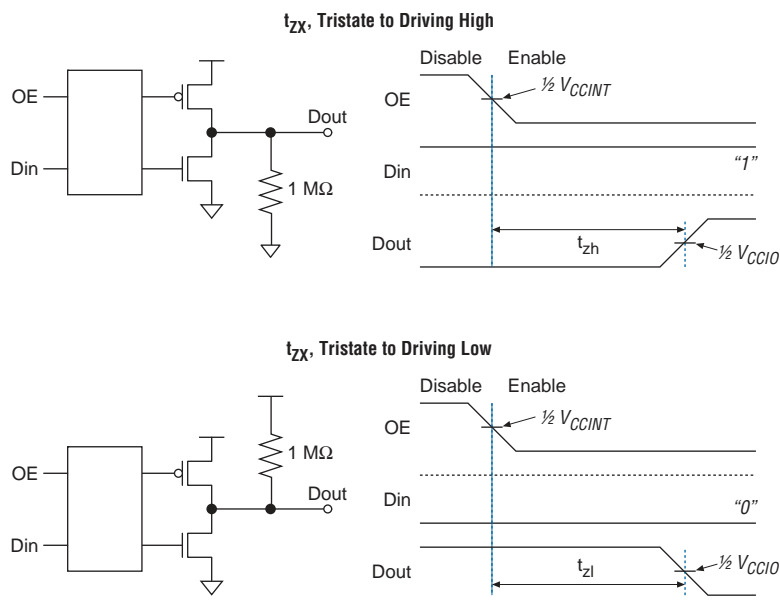


Table 4–54 specifies the input timing measurement setup.

| I/O Standard | Measurement Conditions | | | Measurement Point |
|--------------------|------------------------|---------------|----------------|-------------------|
| | V_{CCIO} (V) | V_{REF} (V) | Edge Rate (ns) | VMEAS (V) |
| LVTTTL (5) | 3.135 | | 3.135 | 1.5675 |
| LVC MOS (5) | 3.135 | | 3.135 | 1.5675 |
| 2.5 V (5) | 2.375 | | 2.375 | 1.1875 |
| 1.8 V (5) | 1.710 | | 1.710 | 0.855 |
| 1.5 V (5) | 1.425 | | 1.425 | 0.7125 |
| PCI (6) | 2.970 | | 2.970 | 1.485 |
| PCI-X (6) | 2.970 | | 2.970 | 1.485 |
| SSTL-2 Class I | 2.325 | 1.163 | 2.325 | 1.1625 |
| SSTL-2 Class II | 2.325 | 1.163 | 2.325 | 1.1625 |
| SSTL-18 Class I | 1.660 | 0.830 | 1.660 | 0.83 |
| SSTL-18 Class II | 1.660 | 0.830 | 1.660 | 0.83 |
| 1.8-V HSTL Class I | 1.660 | 0.830 | 1.660 | 0.83 |

Table 4–54. Timing Measurement Methodology for Input Pins (Part 2 of 2) Notes (1), (2), (3), (4)

| I/O Standard | Measurement Conditions | | | Measurement Point |
|----------------------------------|------------------------|---------------|----------------|-------------------|
| | V_{CCIO} (V) | V_{REF} (V) | Edge Rate (ns) | VMEAS (V) |
| 1.8-V HSTL Class II | 1.660 | 0.830 | 1.660 | 0.83 |
| 1.5-V HSTL Class I | 1.375 | 0.688 | 1.375 | 0.6875 |
| 1.5-V HSTL Class II | 1.375 | 0.688 | 1.375 | 0.6875 |
| 1.2-V HSTL with OCT | 1.140 | 0.570 | 1.140 | 0.570 |
| Differential SSTL-2 Class I | 2.325 | 1.163 | 2.325 | 1.1625 |
| Differential SSTL-2 Class II | 2.325 | 1.163 | 2.325 | 1.1625 |
| Differential SSTL-18 Class I | 1.660 | 0.830 | 1.660 | 0.83 |
| Differential SSTL-18 Class II | 1.660 | 0.830 | 1.660 | 0.83 |
| 1.5-V differential HSTL Class I | 1.375 | 0.688 | 1.375 | 0.6875 |
| 1.5-V differential HSTL Class II | 1.375 | 0.688 | 1.375 | 0.6875 |
| 1.8-V differential HSTL Class I | 1.660 | 0.830 | 1.660 | 0.83 |
| 1.8-V differential HSTL Class II | 1.660 | 0.830 | 1.660 | 0.83 |
| LVDS | 2.325 | | 0.100 | 1.1625 |
| LVPECL | 3.135 | | 0.100 | 1.5675 |

Notes to Table 4–54:

- (1) Input buffer sees no load at buffer input.
- (2) Input measuring point at buffer input is $0.5 V_{CCIO}$.
- (3) Output measuring point is $0.5 V_{CC}$ at internal node.
- (4) Input edge rate is 1 V/ns.
- (5) Less than 50-mV ripple on V_{CCIO} and V_{CCPD} , $V_{CCINT} = 1.15$ V with less than 30-mV ripple.
- (6) $V_{CCPD} = 2.97$ V, less than 50-mV ripple on V_{CCIO} and V_{CCPD} , $V_{CCINT} = 1.15$ V.

Table 4–55 shows the Stratix II GX performance for some common designs. All performance values were obtained with the Quartus II software compilation of LPM or MegaCore functions for FIR and FFT designs.

| Applications | | Resources Used | | | Performance | | | | |
|------------------------------------|----------------------------------|----------------|-------------------------|------------|--------------------|--------------------|----------------|----------------|-------|
| | | ALUTs | TriMatrix Memory Blocks | DSP Blocks | -3 Speed Grade (2) | -3 Speed Grade (3) | -4 Speed Grade | -5 Speed Grade | Units |
| LE | 16-to-1 multiplexer (4) | 21 | 0 | 0 | 657.03 | 620.73 | 589.62 | 477.09 | MHz |
| | 32-to-1 multiplexer (4) | 38 | 0 | 0 | 534.75 | 517.33 | 472.81 | 369.27 | MHz |
| | 16-bit counter | 16 | 0 | 0 | 568.18 | 539.66 | 507.61 | 422.47 | MHz |
| | 64-bit counter | 64 | 0 | 0 | 242.54 | 231.0 | 217.77 | 180.31 | MHz |
| TriMatrix Memory M512 block | Simple dual-port RAM 32 x 18bit | 0 | 1 | 0 | 500.0 | 476.19 | 447.22 | 373.13 | MHz |
| | FIFO 32 x 18 bit | 22 | 1 | 0 | 500.00 | 476.19 | 460.82 | 373.13 | MHz |
| TriMatrix Memory M4K block | Simple dual-port RAM 128 x 36bit | 0 | 1 | 0 | 540.54 | 515.46 | 483.09 | 401.6 | MHz |
| | True dual-port RAM 128 x 18bit | 0 | 1 | 0 | 540.54 | 515.46 | 483.09 | 401.6 | MHz |
| | FIFO 128 x 36 bit | 22 | 1 | 0 | 524.10 | 500.25 | 466.41 | 381.38 | MHz |

Table 4–55. Stratix II GX Performance Notes (Part 2 of 3) *Note (1)*

| Applications | | Resources Used | | | Performance | | | | |
|--------------------------------|-----------------------------------|----------------|-------------------------|------------|--------------------|--------------------|----------------|----------------|-------|
| | | ALUTs | TriMatrix Memory Blocks | DSP Blocks | -3 Speed Grade (2) | -3 Speed Grade (3) | -4 Speed Grade | -5 Speed Grade | Units |
| TriMatrix Memory MegaRAM block | Single port RAM 4K x 144bit | 0 | 1 | 0 | 349.65 | 333.33 | 313.47 | 261.09 | MHz |
| | Simple dual-port RAM 4K x 144bit | 0 | 1 | 0 | 420.16 | 400.0 | 375.93 | 313.47 | MHz |
| | True dual-port RAM 4K x 144 bit | 0 | 1 | 0 | 349.65 | 333.33 | 313.47 | 261.09 | MHz |
| | Single port RAM 8K x 72 bit | 0 | 1 | 0 | 354.6 | 337.83 | 317.46 | 263.85 | MHz |
| | Simple dual-port RAM 8K x 72 bit | 0 | 1 | 0 | 420.16 | 400.0 | 375.93 | 313.47 | MHz |
| | True dual-port RAM 8K x 72 bit | 0 | 1 | 0 | 349.65 | 333.33 | 313.47 | 261.09 | MHz |
| | Single port RAM 16K x 36 bit | 0 | 1 | 0 | 364.96 | 347.22 | 325.73 | 271.73 | MHz |
| | Simple dual-port RAM 16K x 36 bit | 0 | 1 | 0 | 420.16 | 400.0 | 375.93 | 313.47 | MHz |
| | True dual-port RAM 16K x 36 bit | 0 | 1 | 0 | 359.71 | 342.46 | 322.58 | 268.09 | MHz |
| | Single port RAM 32K x 18 bit | 0 | 1 | 0 | 364.96 | 347.22 | 325.73 | 271.73 | MHz |
| | Simple dual-port RAM 32K x 18 bit | 0 | 1 | 0 | 420.16 | 400.0 | 375.93 | 313.47 | MHz |
| | True dual-port RAM 32K x 18 bit | 0 | 1 | 0 | 359.71 | 342.46 | 322.58 | 268.09 | MHz |

| Table 4–55. Stratix II GX Performance Notes (Part 3 of 3) <i>Note (1)</i> | | | | | | | | | |
|--|-----------------------------------|----------------|-------------------------|------------|---------------------------|---------------------------|----------------|----------------|-------|
| Applications | | Resources Used | | | Performance | | | | |
| | | ALUTs | TriMatrix Memory Blocks | DSP Blocks | -3 Speed Grade <i>(2)</i> | -3 Speed Grade <i>(3)</i> | -4 Speed Grade | -5 Speed Grade | Units |
| TriMatrix Memory MegaRAM block (cont.) | Single port RAM 64K x 9 bit | 0 | 1 | 0 | 364.96 | 347.22 | 325.73 | 271.73 | MHz |
| | Simple dual-port RAM 64K x 9 bit | 0 | 1 | 0 | 420.16 | 400.0 | 375.93 | 313.47 | MHz |
| | True dual-port RAM 64K x 9 bit | 0 | 1 | 0 | 359.71 | 342.46 | 322.58 | 268.09 | MHz |
| DSP block | 9 x 9-bit multiplier <i>(5)</i> | 0 | 0 | 1 | 430.29 | 409.16 | 385.2 | 320.1 | MHz |
| | 18 x 18-bit multiplier <i>(5)</i> | 0 | 0 | 1 | 410.17 | 390.01 | 367.1 | 305.06 | MHz |
| | 18 x 18-bit multiplier <i>(7)</i> | 0 | 0 | 1 | 450.04 | 428.08 | 403.22 | 335.12 | MHz |
| | 36 x 36-bit multiplier <i>(5)</i> | 0 | 0 | 1 | 250.0 | 238.15 | 224.01 | 186.6 | MHz |
| | 36 x 36-bit multiplier <i>(6)</i> | 0 | 0 | 1 | 410.17 | 390.01 | 367.1 | 305.06 | MHz |
| | 18-bit, 4-tap FIR filter | 0 | 0 | 1 | 410.17 | 390.01 | 367.1 | 305.06 | MHz |

Notes to Table 4–55:

- (1) These design performance numbers were obtained using the Quartus II software.
- (2) This column refers to -3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
- (3) This column refers to -3 speed grades for EP2SGX130 devices.
- (4) This application uses registered inputs and outputs.
- (5) This application uses registered multiplier input and output stages within the DSP block.
- (6) This application uses registered multiplier input, pipeline, and output stages within the DSP block.
- (7) This application uses registered multiplier inputs with outputs of the multiplier stage feeding the accumulator or subtractor within the DSP block.

Internal Timing Parameters

Refer to Tables 4-56 through 4-61 for internal timing parameters.

| Symbol | Parameter | -3 Speed Grade (1) | | -3 Speed Grade (2) | | -4 Speed Grade | | -5 Speed Grade | | Unit |
|-------------|-------------------------------------|--------------------|-----|--------------------|-----|----------------|-----|----------------|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{SU} | LE register setup time before clock | 90 | | 95 | | 101 | | 121 | | ps |
| t_H | LE register hold time after clock | 149 | | 157 | | 167 | | 200 | | ps |
| t_{CO} | LE register clock-to-output delay | 62 | 94 | 62 | 99 | 62 | 105 | 62 | 127 | ps |
| t_{CLR} | Minimum clear pulse width | 204 | | 214 | | 227 | | 273 | | ps |
| t_{PRE} | Minimum preset pulse width | 204 | | 214 | | 227 | | 273 | | ps |
| t_{CLKL} | Minimum clock low time | 612 | | 642 | | 683 | | 820 | | ps |
| t_{CLKH} | Minimum clock high time | 612 | | 642 | | 683 | | 820 | | ps |
| t_{LUT} | | 170 | 378 | 170 | 397 | 170 | 422 | 170 | 507 | |
| t_{ADDER} | | 372 | 619 | 372 | 650 | 372 | 691 | 372 | 829 | |

Notes to Table 4-56:

- (1) This column refers to -3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
- (2) This column refers to -3 speed grades for EP2SGX130 devices.

| Symbol | Parameter | -3 Speed Grade (1) | | -3 Speed Grade (2) | | -4 Speed Grade | | -5 Speed Grade | | Unit |
|----------|---|--------------------|-----|--------------------|-----|----------------|-----|----------------|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{SU} | IOE input and output register setup time before clock | 122 | | 128 | | 136 | | 163 | | ps |
| t_H | IOE input and output register hold time after clock | 72 | | 75 | | 80 | | 96 | | ps |
| t_{CO} | IOE input and output register clock-to-output delay | 101 | 169 | 101 | 177 | 101 | 188 | 101 | 226 | ps |

Table 4–57. IOE Internal Timing Microparameters (Part 2 of 2)

| Symbol | Parameter | -3 Speed Grade (1) | | -3 Speed Grade (2) | | -4 Speed Grade | | -5 Speed Grade | | Unit |
|----------------------|---|--------------------|------|--------------------|------|----------------|------|----------------|------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{PIN2COMBOUT_R}$ | Row input pin to IOE combinational output | 410 | 760 | 410 | 798 | 410 | 848 | 410 | 1018 | ps |
| $t_{PIN2COMBOUT_C}$ | Column input pin to IOE combinational output | 428 | 787 | 428 | 825 | 428 | 878 | 428 | 1054 | ps |
| $t_{COMBIN2PIN_R}$ | Row IOE data input to combinational output pin | 1101 | 2026 | 1101 | 2127 | 1101 | 2261 | 1101 | 2439 | ps |
| $t_{COMBIN2PIN_C}$ | Column IOE data input to combinational output pin | 991 | 1854 | 991 | 1946 | 991 | 2069 | 991 | 2246 | ps |
| t_{CLR} | Minimum clear pulse width | 200 | | 210 | | 223 | | 268 | | ps |
| t_{PRE} | Minimum preset pulse width | 200 | | 210 | | 223 | | 268 | | ps |
| t_{CLKL} | Minimum clock low time | 600 | | 630 | | 669 | | 804 | | ps |
| t_{CLKH} | Minimum clock high time | 600 | | 630 | | 669 | | 804 | | ps |

(1) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.

(2) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–58. DSP Block Internal Timing Microparameters (Part 1 of 2)

| Symbol | Parameter | -3 Speed Grade (1) | | -3 Speed Grade (2) | | -4 Speed Grade | | -5 Speed Grade | | Unit |
|----------|--|--------------------|-----|--------------------|-----|----------------|-----|----------------|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{SU} | Input, pipeline, and output register setup time before clock | 50 | | 52 | | 55 | | 67 | | ps |
| t_{H} | Input, pipeline, and output register hold time after clock | 180 | | 189 | | 200 | | 241 | | ps |
| t_{CO} | Input, pipeline, and output register clock-to-output delay | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ps |

Table 4–58. DSP Block Internal Timing Microparameters (Part 2 of 2)

| Symbol | Parameter | -3 Speed Grade (1) | | -3 Speed Grade (2) | | -4 Speed Grade | | -5 Speed Grade | | Unit |
|-----------------------|---|--------------------|------|--------------------|------|----------------|------|----------------|------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{INREG2PIPE9}$ | Input register to DSP block pipeline register in 9 × 9-bit mode | 1312 | 2030 | 1312 | 2131 | 1312 | 2266 | 1312 | 2720 | ps |
| $t_{INREG2PIPE18}$ | Input register to DSP block pipeline register in 18 × 18-bit mode | 1302 | 2010 | 1302 | 2110 | 1302 | 2244 | 1302 | 2693 | ps |
| $t_{INREG2PIPE36}$ | Input register to DSP block pipeline register in 36 × 36-bit mode | 1302 | 2010 | 1302 | 2110 | 1302 | 2244 | 1302 | 2693 | ps |
| $t_{PIPE2OUTREG2ADD}$ | DSP block pipeline register to output register delay in two-multipliers adder mode | 924 | 1450 | 924 | 1522 | 924 | 1618 | 924 | 1943 | ps |
| $t_{PIPE2OUTREG4ADD}$ | DSP block pipeline register to output register delay in four-multipliers adder mode | 1134 | 1850 | 1134 | 1942 | 1134 | 2065 | 1134 | 2479 | ps |
| t_{PD9} | Combinational input to output delay for 9 × 9 | 2100 | 2880 | 2100 | 3024 | 2100 | 3214 | 2100 | 3859 | ps |
| t_{PD18} | Combinational input to output delay for 18 × 18 | 2110 | 2990 | 2110 | 3139 | 2110 | 3337 | 2110 | 4006 | ps |
| t_{PD36} | Combinational input to output delay for 36 × 36 | 2939 | 4450 | 2939 | 4672 | 2939 | 4967 | 2939 | 5962 | ps |
| t_{CLR} | Minimum clear pulse width | 2212 | | 2322 | | 2469 | | 2964 | | ps |
| t_{CLKL} | Minimum clock low time | 1190 | | 1249 | | 1328 | | 1594 | | ps |
| t_{CLKH} | Minimum clock high time | 1190 | | 1249 | | 1328 | | 1594 | | ps |

(1) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.

(2) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–59. M512 Block Internal Timing Microparameters (Part 1 of 2)

| Symbol | Parameter | -3 Speed Grade ⁽²⁾ | | -3 Speed Grade ⁽³⁾ | | -4 Speed Grade | | -5 Speed Grade | | Unit |
|-------------------|---|-------------------------------|------|-------------------------------|------|----------------|------|----------------|------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{M512RC} | Synchronous read cycle time | 2089 | 2318 | 2089 | 2433 | 2089 | 2587 | 2089 | 3104 | ps |
| $t_{M512WERESU}$ | Write or read enable setup time before clock | 22 | | 23 | | 24 | | 29 | | ps |
| $t_{M512WEREH}$ | Write or read enable hold time after clock | 203 | | 213 | | 226 | | 272 | | ps |
| $t_{M512DATASU}$ | Data setup time before clock | 22 | | 23 | | 24 | | 29 | | ps |
| $t_{M512DATAH}$ | Data hold time after clock | 203 | | 213 | | 226 | | 272 | | ps |
| $t_{M512WADDRSU}$ | Write address setup time before clock | 22 | | 23 | | 24 | | 29 | | ps |
| $t_{M512WADDRH}$ | Write address hold time after clock | 203 | | 213 | | 226 | | 272 | | ps |
| $t_{M512RADDRSU}$ | Read address setup time before clock | 22 | | 23 | | 24 | | 29 | | ps |
| $t_{M512RADDRH}$ | Read address hold time after clock | 203 | | 213 | | 226 | | 272 | | ps |
| $t_{M512DATACO1}$ | Clock-to-output delay when using output registers | 298 | 478 | 298 | 501 | 298 | 533 | 298 | 640 | ps |
| $t_{M512DATACO2}$ | Clock-to-output delay without output registers | 2102 | 2345 | 2102 | 2461 | 2102 | 2616 | 2102 | 3141 | ps |
| $t_{M512CLKL}$ | Minimum clock low time | 1315 | | 1380 | | 1468 | | 1762 | | ps |
| $t_{M512CLKH}$ | Minimum clock high time | 1315 | | 1380 | | 1468 | | 1762 | | ps |

Table 4–59. M512 Block Internal Timing Microparameters (Part 2 of 2)

| Symbol | Parameter | -3 Speed Grade ⁽²⁾ | | -3 Speed Grade ⁽³⁾ | | -4 Speed Grade | | -5 Speed Grade | | Unit |
|---------------|---------------------------|-------------------------------|-----|-------------------------------|-----|----------------|-----|----------------|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{M512CLR}$ | Minimum clear pulse width | 144 | | 151 | | 160 | | 192 | | ps |

- (1) The M512 block f_{MAX} obtained using the Quartus II software does not necessarily equal to 1/TM512RC.
(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(3) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–60. M4K Block Internal Timing Microparameters (Part 1 of 2) *Note (1)*

| Symbol | Parameter | -3 Speed Grade ⁽²⁾ | | -3 Speed Grade ⁽³⁾ | | -4 Speed Grade | | -5 Speed Grade | | Unit |
|------------------|--|-------------------------------|------|-------------------------------|------|----------------|------|----------------|------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{M4KRC} | Synchronous read cycle time | 1462 | 2240 | 1462 | 2351 | 1462 | 2500 | 1462 | 3000 | ps |
| $t_{M4KWRESU}$ | Write or read enable setup time before clock | 22 | | 23 | | 24 | | 29 | | ps |
| $t_{M4KWREH}$ | Write or read enable hold time after clock | 203 | | 213 | | 226 | | 272 | | ps |
| $t_{M4KBESU}$ | Byte enable setup time before clock | 22 | | 23 | | 24 | | 29 | | ps |
| t_{M4KBEH} | Byte enable hold time after clock | 203 | | 213 | | 226 | | 272 | | ps |
| $t_{M4KDATAASU}$ | A port data setup time before clock | 22 | | 23 | | 24 | | 29 | | ps |
| $t_{M4KDATAAH}$ | A port data hold time after clock | 203 | | 213 | | 226 | | 272 | | ps |
| $t_{M4KADDRASU}$ | A port address setup time before clock | 22 | | 23 | | 24 | | 29 | | ps |
| $t_{M4KADDRAH}$ | A port address hold time after clock | 203 | | 213 | | 226 | | 272 | | ps |
| $t_{M4KDATABSU}$ | B port data setup time before clock | 22 | | 23 | | 24 | | 29 | | ps |

| Symbol | Parameter | -3 Speed Grade (2) | | -3 Speed Grade (3) | | -4 Speed Grade | | -5 Speed Grade | | Unit |
|-------------------|---|-----------------------|------|-----------------------|------|----------------|------|----------------|------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{M4KDATA BH}$ | B port data hold time after clock | 203 | | 213 | | 226 | | 272 | | ps |
| $t_{M4KRADDRBSU}$ | B port address setup time before clock | 22 | | 23 | | 24 | | 29 | | ps |
| $t_{M4KRADDRBH}$ | B port address hold time after clock | 203 | | 213 | | 226 | | 272 | | ps |
| $t_{M4KDATA CO1}$ | Clock-to-output delay when using output registers | 334 | 524 | 334 | 549 | 334 | 584 | 334 | 701 | ps |
| $t_{M4KDATA CO2}$ | Clock-to-output delay without output registers | 1616 | 2453 | 1616 | 2574 | 1616 | 2737 | 1616 | 3286 | ps |
| $t_{M4KCLKH}$ | Minimum clock high time | 1250 | | 1312 | | 1395 | | 1675 | | ps |
| $t_{M4KCLKL}$ | Minimum clock low time | 1250 | | 1312 | | 1395 | | 1675 | | ps |
| t_{M4KCLR} | Minimum clear pulse width | 144 | | 151 | | 160 | | 192 | | ps |

(1) The M512 block f_{MAX} obtained using the Quartus II software does not necessarily equal to $1/TM4KRC$.

(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.

(3) This column refers to –3 speed grades for EP2SGX130 devices.

| Symbol | Parameter | -3 Speed Grade (2) | | -3 Speed Grade (3) | | -4 Speed Grade | | -5 Speed Grade | | Unit |
|------------------|--|-----------------------|------|-----------------------|------|----------------|------|----------------|------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{MEGARC} | Synchronous read cycle time | 1866 | 2774 | 1866 | 2911 | 1866 | 3096 | 1866 | 3716 | ps |
| $t_{MEGAWERESU}$ | Write or read enable setup time before clock | 144 | | 151 | | 160 | | 192 | | ps |
| $t_{MEGAWEREH}$ | Write or read enable hold time after clock | 39 | | 40 | | 43 | | 52 | | ps |

Table 4–61. M-RAM Block Internal Timing Microparameters (Part 2 of 2) *Note (1)*

| Symbol | Parameter | -3 Speed Grade (2) | | -3 Speed Grade (3) | | -4 Speed Grade | | -5 Speed Grade | | Unit |
|--------------------------|---|--------------------|------|--------------------|------|----------------|------|----------------|------|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{MEGABESU} | Byte enable setup time before clock | -9 | | -10 | | -11 | | -13 | | ps |
| t_{MEGABEH} | Byte enable hold time after clock | 39 | | 40 | | 43 | | 52 | | ps |
| $t_{\text{MEGADATAASU}}$ | A port data setup time before clock | 50 | | 52 | | 55 | | 67 | | ps |
| $t_{\text{MEGADATAAH}}$ | A port data hold time after clock | 243 | | 255 | | 271 | | 325 | | ps |
| $t_{\text{MEGAADDRASU}}$ | A port address setup time before clock | 589 | | 618 | | 657 | | 789 | | ps |
| $t_{\text{MEGAADDRAH}}$ | A port address hold time after clock | -347 | | -365 | | -388 | | -465 | | ps |
| $t_{\text{MEGADATABSU}}$ | B port setup time before clock | 50 | | 52 | | 55 | | 67 | | ps |
| $t_{\text{MEGADATABH}}$ | B port hold time after clock | 243 | | 255 | | 271 | | 325 | | ps |
| $t_{\text{MEGAADDRBSU}}$ | B port address setup time before clock | 589 | | 618 | | 657 | | 789 | | ps |
| $t_{\text{MEGAADDRBH}}$ | B port address hold time after clock | -347 | | -365 | | -388 | | -465 | | ps |
| $t_{\text{MEGADATACO1}}$ | Clock-to-output delay when using output registers | 480 | 715 | 480 | 749 | 480 | 797 | 480 | 957 | ps |
| $t_{\text{MEGADATACO2}}$ | Clock-to-output delay without output registers | 1950 | 2899 | 1950 | 3042 | 1950 | 3235 | 1950 | 3884 | ps |
| t_{MEGACLKL} | Minimum clock low time | 1250 | | 1312 | | 1395 | | 1675 | | ps |
| t_{MEGACLKH} | Minimum clock high time | 1250 | | 1312 | | 1395 | | 1675 | | ps |
| t_{MEGACLR} | Minimum clear pulse width | 144 | | 151 | | 160 | | 192 | | ps |

(1) The M512 block f_{MAX} obtained using the Quartus II software does not necessarily equal to $1/\text{TMEGARC}$.

(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.

(3) This column refers to –3 speed grades for EP2SGX130 devices.

Stratix II GX Clock Timing Parameters

See Tables 4–62 through 4–78 for Stratix II GX clock timing parameters.

| Symbol | Parameter |
|----------------------|---|
| t_{CIN} | Delay from clock pad to I/O input register |
| t_{COUT} | Delay from clock pad to I/O output register |
| t_{PLLCIN} | Delay from PLL inclk pad to I/O input register |
| t_{PLLCOUT} | Delay from PLL inclk pad to I/O output register |

EP2SGX30 Clock Timing Parameters

Tables 4–63 through 4–66 show the maximum clock timing parameters for EP2SGX30 devices.

| Parameter | Fast Corner | | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Units |
|----------------------|-------------|------------|----------------|----------------|----------------|-------|
| | Industrial | Commercial | | | | |
| t_{CIN} | 1.615 | 1.633 | 2.669 | 2.968 | 3.552 | ns |
| t_{COUT} | 1.450 | 1.468 | 2.427 | 2.698 | 3.228 | ns |
| t_{PLLCIN} | 0.11 | 0.129 | 0.428 | 0.466 | 0.547 | ns |
| t_{PLLCOUT} | -0.055 | -0.036 | 0.186 | 0.196 | 0.223 | ns |

| Parameter | Fast Corner | | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Units |
|----------------------|-------------|------------|----------------|----------------|----------------|-------|
| | Industrial | Commercial | | | | |
| t_{CIN} | 1.365 | 1.382 | 2.280 | 2.535 | 3.033 | ns |
| t_{COUT} | 1.370 | 1.387 | 2.276 | 2.531 | 3.028 | ns |
| t_{PLLCIN} | -0.151 | -0.136 | 0.043 | 0.037 | 0.032 | ns |
| t_{PLLCOUT} | -0.146 | -0.131 | 0.039 | 0.033 | 0.027 | ns |

Table 4–65. EP2SGX30 Column Pins Regional Clock Timing Parameters

| Parameter | Fast Corner | | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Units |
|---------------|-------------|------------|----------------|----------------|----------------|-------|
| | Industrial | Commercial | | | | |
| t_{CIN} | 1.493 | 1.507 | 2.522 | 2.806 | 3.364 | ns |
| t_{COUT} | 1.353 | 1.372 | 2.525 | 2.809 | 3.364 | ns |
| t_{PLLCIN} | 0.087 | 0.104 | 0.237 | 0.253 | 0.292 | ns |
| $t_{PLLCOUT}$ | -0.078 | -0.061 | 0.237 | 0.253 | 0.29 | ns |

Table 4–66. EP2SGX30 Row Pins Regional Clock Timing Parameters

| Parameter | Fast Corner | | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Units |
|---------------|-------------|------------|----------------|----------------|----------------|-------|
| | Industrial | Commercial | | | | |
| t_{CIN} | 1.246 | 1.262 | 2.437 | 2.712 | 3.246 | ns |
| t_{COUT} | 1.251 | 1.267 | 2.437 | 2.712 | 3.246 | ns |
| t_{PLLCIN} | -0.18 | -0.167 | 0.215 | 0.229 | 0.263 | ns |
| $t_{PLLCOUT}$ | -0.175 | -0.162 | 0.215 | 0.229 | 0.263 | ns |

EP2SGX60 Clock Timing Parameters

Tables 4–67 through 4–70 show the maximum clock timing parameters for EP2SGX60 devices.

Table 4–67. EP2SGX60 Column Pins Global Clock Timing Parameters

| Parameter | Fast Corner | | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Units |
|---------------|-------------|------------|----------------|----------------|----------------|-------|
| | Industrial | Commercial | | | | |
| t_{CIN} | 1.722 | 1.736 | 2.940 | 3.275 | 3.919 | ns |
| t_{COUT} | 1.557 | 1.571 | 2.698 | 3.005 | 3.595 | ns |
| t_{PLLCIN} | 0.037 | 0.051 | 0.474 | 0.521 | 0.613 | ns |
| $t_{PLLCOUT}$ | -0.128 | -0.114 | 0.232 | 0.251 | 0.289 | ns |

Table 4–68. EP2SGX60 Row Pins Global Clock Timing Parameters

| Parameter | Fast Corner | | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Units |
|---------------|-------------|------------|----------------|----------------|----------------|-------|
| | Industrial | Commercial | | | | |
| t_{CIN} | 1.494 | 1.508 | 2.582 | 2.875 | 3.441 | ns |
| t_{COUT} | 1.499 | 1.513 | 2.578 | 2.871 | 3.436 | ns |
| t_{PLLCIN} | -0.183 | -0.168 | 0.116 | 0.122 | 0.135 | ns |
| $t_{PLLCOUT}$ | -0.178 | -0.163 | 0.112 | 0.118 | 0.13 | ns |

Table 4–69. EP2SGX60 Column Pins Regional Clock Timing Parameters

| Parameter | Fast Corner | | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Units |
|---------------|-------------|------------|----------------|----------------|----------------|-------|
| | Industrial | Commercial | | | | |
| t_{CIN} | 1.577 | 1.591 | 2.736 | 3.048 | 3.648 | ns |
| t_{COUT} | 1.412 | 1.426 | 2.740 | 3.052 | 3.653 | ns |
| t_{PLLCIN} | 0.065 | 0.08 | 0.334 | 0.361 | 0.423 | ns |
| $t_{PLLCOUT}$ | -0.1 | -0.085 | 0.334 | 0.361 | 0.423 | ns |

Table 4–70. EP2SGX60 Row Pins Regional Clock Timing Parameters

| Parameter | Fast Corner | | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Units |
|---------------|-------------|------------|----------------|----------------|----------------|-------|
| | Industrial | Commercial | | | | |
| t_{CIN} | 1.342 | 1.355 | 2.716 | 3.024 | 3.622 | ns |
| t_{COUT} | 1.347 | 1.360 | 2.716 | 3.024 | 3.622 | ns |
| t_{PLLCIN} | -0.18 | -0.166 | 0.326 | 0.352 | 0.412 | ns |
| $t_{PLLCOUT}$ | -0.175 | -0.161 | 0.334 | 0.361 | 0.423 | ns |

EP2SGX90 Clock Timing Parameters

Tables 4–71 through 4–74 show the maximum clock timing parameters for EP2SGX90 devices.

Table 4–71. EP2SGX90 Column Pins Global Clock Timing Parameters

| Parameter | Fast Corner | | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Units |
|---------------|-------------|------------|----------------|----------------|----------------|-------|
| | Industrial | Commercial | | | | |
| t_{CIN} | 1.861 | 1.878 | 3.115 | 3.465 | 4.143 | ns |
| t_{COUT} | 1.696 | 1.713 | 2.873 | 3.195 | 3.819 | ns |
| t_{PLLCIN} | -0.254 | -0.237 | 0.171 | 0.179 | 0.206 | ns |
| $t_{PLLCOUT}$ | -0.419 | -0.402 | -0.071 | -0.091 | -0.118 | ns |

Table 4–72. EP2SGX90 Row Pins Global Clock Timing Parameters

| Parameter | Fast Corner | | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Units |
|---------------|-------------|------------|----------------|----------------|----------------|-------|
| | Industrial | Commercial | | | | |
| t_{CIN} | 1.634 | 1.650 | 2.768 | 3.076 | 3.678 | ns |
| t_{COUT} | 1.639 | 1.655 | 2.764 | 3.072 | 3.673 | ns |
| t_{PLLCIN} | -0.481 | -0.465 | -0.189 | -0.223 | -0.279 | ns |
| $t_{PLLCOUT}$ | -0.476 | -0.46 | -0.193 | -0.227 | -0.284 | ns |

Table 4–73. EP2SGX90 Column Pins Regional Clock Timing Parameters

| Parameter | Fast Corner | | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Units |
|---------------|-------------|------------|----------------|----------------|----------------|-------|
| | Industrial | Commercial | | | | |
| t_{CIN} | 1.688 | 1.702 | 2.896 | 3.224 | 3.856 | ns |
| t_{COUT} | 1.551 | 1.569 | 2.893 | 3.220 | 3.851 | ns |
| t_{PLLCIN} | -0.105 | -0.089 | 0.224 | 0.241 | 0.254 | ns |
| $t_{PLLCOUT}$ | -0.27 | -0.254 | 0.224 | 0.241 | 0.254 | ns |

Table 4–74. EP2SGX90 Row Pins Regional Clock Timing Parameters

| Parameter | Fast Corner | | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Units |
|---------------|-------------|------------|----------------|----------------|----------------|-------|
| | Industrial | Commercial | | | | |
| t_{CIN} | 1.444 | 1.461 | 2.792 | 3.108 | 3.716 | ns |
| t_{COUT} | 1.449 | 1.466 | 2.792 | 3.108 | 3.716 | ns |
| t_{PLLCIN} | -0.348 | -0.333 | 0.204 | 0.217 | 0.243 | ns |
| $t_{PLLCOUT}$ | -0.343 | -0.328 | 0.212 | 0.217 | 0.254 | ns |

EP2SGX130 Clock Timing Parameters

Tables 4–75 through 4–78 show the maximum clock timing parameters for EP2SGX130 devices.

Table 4–75. EP2SGX130 Column Pins Global Clock Timing Parameters

| Parameter | Fast Corner | | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Units |
|---------------|-------------|------------|----------------|----------------|----------------|-------|
| | Industrial | Commercial | | | | |
| t_{CIN} | 1.980 | 1.998 | 3.491 | 3.706 | 4.434 | ns |
| t_{COUT} | 1.815 | 1.833 | 3.237 | 3.436 | 4.110 | ns |
| t_{PLLCIN} | -0.027 | -0.009 | 0.307 | 0.322 | 0.376 | ns |
| $t_{PLLCOUT}$ | -0.192 | -0.174 | 0.053 | 0.052 | 0.052 | ns |

Table 4–76. EP2SGX130 Row Pins Global Clock Timing Parameters

| Parameter | Fast Corner | | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Units |
|---------------|-------------|------------|----------------|----------------|----------------|-------|
| | Industrial | Commercial | | | | |
| t_{CIN} | 1.741 | 1.759 | 3.112 | 3.303 | 3.950 | ns |
| t_{COUT} | 1.746 | 1.764 | 3.108 | 3.299 | 3.945 | ns |
| t_{PLLCIN} | -0.261 | -0.243 | -0.089 | -0.099 | -0.129 | ns |
| $t_{PLLCOUT}$ | -0.256 | -0.238 | -0.093 | -0.103 | -0.134 | ns |

Table 4–77. EP2SGX130 Column Pins Regional Clock Timing Parameters

| Parameter | Fast Corner | | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Units |
|-----------------|-------------|------------|----------------|----------------|----------------|-------|
| | Industrial | Commercial | | | | |
| t_{CIN} | 1.815 | 1.834 | 3.218 | 3.417 | 4.087 | ns |
| t_{COUT} | 1.650 | 1.669 | 3.218 | 3.417 | 4.087 | ns |
| $t_{PLL\,CIN}$ | 0.116 | 0.134 | 0.349 | 0.364 | 0.426 | ns |
| $t_{PLL\,COUT}$ | -0.049 | -0.031 | 0.361 | 0.378 | 0.444 | ns |

Table 4–78. EP2SGX130 Row Pins Regional Clock Timing Parameters

| Parameter | Fast Corner | | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Units |
|-----------------|-------------|------------|----------------|----------------|----------------|-------|
| | Industrial | Commercial | | | | |
| t_{CIN} | 1.544 | 1.560 | 3.195 | 3.395 | 4.060 | ns |
| t_{COUT} | 1.549 | 1.565 | 3.195 | 3.395 | 4.060 | ns |
| $t_{PLL\,CIN}$ | -0.149 | -0.132 | 0.34 | 0.356 | 0.417 | ns |
| $t_{PLL\,COUT}$ | -0.144 | -0.127 | 0.342 | 0.356 | 0.417 | ns |

Clock Network Skew Adders

The Quartus II software models skew within dedicated clock networks such as global and regional clocks. Therefore, the intra-clock network skew adder is not specified. Table 4–79 specifies the intra-clock skew between any two clock networks driving any registers in the Stratix II GX device.

Table 4–79. Clock Network Specifications (Part 1 of 2)

| Name | Description | Min | Typ | Max | Unit |
|----------------------------------|----------------------------------|-----|-----|------|------|
| Clock skew adder EP2SGX30 (1) | Inter-clock network, same side | | | ±50 | ps |
| | Inter-clock network, entire chip | | | ±100 | ps |
| Clock skew adder EP2SGX60 (1) | Inter-clock network, same side | | | ±50 | ps |
| | Inter-clock network, entire chip | | | ±100 | ps |
| Clock skew adder EP2SGX90 (1) | Inter-clock network, same side | | | ±55 | ps |
| | Inter-clock network, entire chip | | | ±110 | ps |

Table 4–79. Clock Network Specifications (Part 2 of 2)

| Name | Description | Min | Typ | Max | Unit |
|-----------------------------------|----------------------------------|-----|-----|------|------|
| Clock skew adder EP2SGX130 (1) | Inter-clock network, same side | | | ±63 | ps |
| | Inter-clock network, entire chip | | | ±125 | ps |

(1) This is in addition to intra-clock network skew, which is modeled in the Quartus II software.

IOE Programmable Delay

See Tables 4–80 and 4–81 for IOE programmable delay.

Table 4–80. Stratix II GX IOE Programmable Delay on Column Pins *Note (1)*

| Parameter | Paths Affected | Available Settings | Minimum Timing | | -3 Speed Grade (2) | | -3 Speed Grade (3) | | -4 Speed Grade | | -5 Speed Grade | | Unit |
|--|----------------------------|--------------------|----------------|------------|--------------------|------------|--------------------|------------|----------------|------------|----------------|------------|------|
| | | | Min Offset | Max Offset | Min Offset | Max Offset | Min Offset | Max Offset | Min Offset | Max Offset | Min Offset | Max Offset | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 8 | 0 | 1781 | 0 | 2881 | 0 | 3025 | 0 | 3217 | 0 | 3,860 | ps |
| Input delay from pin to input register | Pad to I/O input register | 64 | 0 | 2053 | 0 | 3275 | 0 | 3439 | 0 | 3657 | 0 | 4388 | ps |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 332 | 0 | 500 | 0 | 525 | 0 | 559 | 0 | 670 | ps |
| Output enable pin delay | t_{xz} , t_{zx} | 2 | 0 | 320 | 0 | 483 | 0 | 507 | 0 | 539 | 0 | 647 | ps |

(1) The incremental values for the settings are generally linear. For the exact delay associated with each setting, use the latest version of the Quartus II software.

(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.

(3) This column refers to –3 speed grades for EP2SGX130 devices.

| Parameter | Paths Affected | Available Settings | Minimum Timing | | -3 Speed Grade | | -3 Speed Grade | | -4 Speed Grade | | -5 Speed Grade | | Unit |
|--|-----------------------------------|--------------------|----------------|------------|----------------|------------|----------------|------------|----------------|------------|----------------|------------|------|
| | | | Min Offset | Max Offset | Min Offset | Max Offset | Min Offset | Max Offset | Min Offset | Max Offset | Min Offset | Max Offset | |
| Input delay from pin to internal cells | Pad to I/O dataout to logic array | 8 | 0 | 1782 | 0 | 2876 | 0 | 3020 | 0 | 3212 | 0 | 3853 | ps |
| Input delay from pin to input register | Pad to I/O input register | 64 | 0 | 2054 | 0 | 3270 | 0 | 3434 | 0 | 3652 | 0 | 4381 | ps |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 332 | 0 | 500 | 0 | 525 | 0 | 559 | 0 | 670 | ps |
| Output enable pin delay | t_{xz} , t_{zx} | 2 | 0 | 320 | 0 | 483 | 0 | 507 | 0 | 539 | 0 | 647 | ps |

- (1) The incremental values for the settings are generally linear. For the exact delay associated with each setting, use the latest version of the Quartus II software.

Default Capacitive Loading of Different I/O Standards

See [Table 4–82](#) for default capacitive loading of different I/O standards.

| I/O Standard | Capacitive Load | Unit |
|-----------------|-----------------|------|
| LVTTTL | 0 | pF |
| LVC MOS | 0 | pF |
| 2.5 V | 0 | pF |
| 1.8 V | 0 | pF |
| 1.5 V | 0 | pF |
| PCI | 10 | pF |
| PCI-X | 10 | pF |
| SSTL-2 Class I | 0 | pF |
| SSTL-2 Class II | 0 | pF |

Table 4–82. Default Loading of Different I/O Standards for Stratix II GX Devices (Part 2 of 2)

| I/O Standard | Capacitive Load | Unit |
|----------------------------------|-----------------|------|
| SSTL-18 Class I | 0 | pF |
| SSTL-18 Class II | 0 | pF |
| 1.5-V HSTL Class I | 0 | pF |
| 1.5-V HSTL Class II | 0 | pF |
| 1.8-V HSTL Class I | 0 | pF |
| 1.8-V HSTL Class II | 0 | pF |
| Differential SSTL-2 Class I | 0 | pF |
| Differential SSTL-2 Class II | 0 | pF |
| Differential SSTL-18 Class I | 0 | pF |
| Differential SSTL-18 Class II | 0 | pF |
| 1.5-V differential HSTL Class I | 0 | pF |
| 1.5-V differential HSTL Class II | 0 | pF |
| 1.8-V differential HSTL Class I | 0 | pF |
| 1.8-V differential HSTL Class II | 0 | pF |
| LVDS | 0 | pF |

I/O Delays

See [Tables 4–83 through 4–87](#) for I/O delays.

Table 4–83. I/O Delay Parameters

| Symbol | Parameter |
|-------------|--|
| t_{DIP} | Delay from I/O datain to output pad |
| t_{OP} | Delay from I/O output register to output pad |
| t_{PCOUT} | Delay from input pad to I/O dataout to core |
| t_{PI} | Delay from input pad to I/O input register |

Table 4–84. Stratix II GX I/O Input Delay for Column Pins (Part 1 of 3)

| I/O Standard | Parameter | Fast Corner Industrial/Commercial | -3 Speed Grade (2) | -3 Speed Grade (3) | -4 Speed Grade | -5 Speed Grade | Unit |
|--------------|-------------|-----------------------------------|--------------------|--------------------|----------------|----------------|------|
| LVTTTL | t_{PI} | 707 | 1223 | 1282 | 1364 | 1637 | ps |
| | t_{PCOUT} | 428 | 787 | 825 | 878 | 1054 | ps |

Table 4–84. Stratix II GX I/O Input Delay for Column Pins (Part 2 of 3)

| I/O Standard | Parameter | Fast Corner Industrial/ Commercial | -3 Speed Grade (2) | -3 Speed Grade (3) | -4 Speed Grade | -5 Speed Grade | Unit |
|---------------------------------|-------------|------------------------------------|--------------------|--------------------|----------------|----------------|------|
| 2.5 V | t_{PI} | 717 | 1210 | 1269 | 1349 | 1619 | ps |
| | t_{PCOUT} | 438 | 774 | 812 | 863 | 1036 | ps |
| 1.8 V | t_{PI} | 783 | 1366 | 1433 | 1523 | 1829 | ps |
| | t_{PCOUT} | 504 | 930 | 976 | 1037 | 1246 | ps |
| 1.5 V | t_{PI} | 786 | 1436 | 1506 | 1602 | 1922 | ps |
| | t_{PCOUT} | 507 | 1000 | 1049 | 1116 | 1339 | ps |
| LVCMOS | t_{PI} | 707 | 1223 | 1282 | 1364 | 1637 | ps |
| | t_{PCOUT} | 428 | 787 | 825 | 878 | 1054 | ps |
| SSTL-2 Class I | t_{PI} | 530 | 818 | 857 | 912 | 1094 | ps |
| | t_{PCOUT} | 251 | 382 | 400 | 426 | 511 | ps |
| SSTL-2 Class II | t_{PI} | 530 | 818 | 857 | 912 | 1094 | ps |
| | t_{PCOUT} | 251 | 382 | 400 | 426 | 511 | ps |
| SSTL-18 Class I | t_{PI} | 569 | 898 | 941 | 1001 | 1201 | ps |
| | t_{PCOUT} | 290 | 462 | 484 | 515 | 618 | ps |
| SSTL-18 Class II | t_{PI} | 569 | 898 | 941 | 1001 | 1201 | ps |
| | t_{PCOUT} | 290 | 462 | 484 | 515 | 618 | ps |
| 1.5-V HSTL Class I | t_{PI} | 587 | 993 | 1041 | 1107 | 1329 | ps |
| | t_{PCOUT} | 308 | 557 | 584 | 621 | 746 | ps |
| 1.5-V HSTL Class II | t_{PI} | 587 | 993 | 1041 | 1107 | 1329 | ps |
| | t_{PCOUT} | 308 | 557 | 584 | 621 | 746 | ps |
| 1.8-V HSTL Class I | t_{PI} | 569 | 898 | 941 | 1001 | 1201 | ps |
| | t_{PCOUT} | 290 | 462 | 484 | 515 | 618 | ps |
| 1.8-V HSTL Class II | t_{PI} | 569 | 898 | 941 | 1001 | 1201 | ps |
| | t_{PCOUT} | 290 | 462 | 484 | 515 | 618 | ps |
| PCI | t_{PI} | 712 | 1214 | 1273 | 1354 | 1625 | ps |
| | t_{PCOUT} | 433 | 778 | 816 | 868 | 1042 | ps |
| PCI-X | t_{PI} | 712 | 1214 | 1273 | 1354 | 1625 | ps |
| | t_{PCOUT} | 433 | 778 | 816 | 868 | 1042 | ps |
| Differential SSTL-2 Class I (1) | t_{PI} | 530 | 818 | 857 | 912 | 1094 | ps |
| | t_{PCOUT} | 251 | 382 | 400 | 426 | 511 | ps |

Table 4–84. Stratix II GX I/O Input Delay for Column Pins (Part 3 of 3)

| I/O Standard | Parameter | Fast Corner Industrial/ Commercial | -3 Speed Grade (2) | -3 Speed Grade (3) | -4 Speed Grade | -5 Speed Grade | Unit |
|--------------------------------------|-------------|------------------------------------|--------------------|--------------------|----------------|----------------|------|
| Differential SSTL-2 Class II (1) | t_{PI} | 530 | 818 | 857 | 912 | 1094 | ps |
| | t_{PCOUT} | 251 | 382 | 400 | 426 | 511 | ps |
| Differential SSTL-18 Class I (1) | t_{PI} | 569 | 898 | 941 | 1001 | 1201 | ps |
| | t_{PCOUT} | 290 | 462 | 484 | 515 | 618 | ps |
| Differential SSTL-18 Class II (1) | t_{PI} | 569 | 898 | 941 | 1001 | 1201 | ps |
| | t_{PCOUT} | 290 | 462 | 484 | 515 | 618 | ps |
| 1.8-V differential HSTL Class I (1) | t_{PI} | 569 | 898 | 941 | 1001 | 1201 | ps |
| | t_{PCOUT} | 290 | 462 | 484 | 515 | 618 | ps |
| 1.8-V differential HSTL Class II (1) | t_{PI} | 569 | 898 | 941 | 1001 | 1201 | ps |
| | t_{PCOUT} | 290 | 462 | 484 | 515 | 618 | ps |
| 1.5-V differential HSTL Class I (1) | t_{PI} | 587 | 993 | 1041 | 1107 | 1329 | ps |
| | t_{PCOUT} | 308 | 557 | 584 | 621 | 746 | ps |
| 1.5-V differential HSTL Class II (1) | t_{PI} | 587 | 993 | 1041 | 1107 | 1329 | ps |
| | t_{PCOUT} | 308 | 557 | 584 | 621 | 746 | ps |

(1) These I/O standards are only supported on DQS pins.

(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.

(3) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–85. Stratix II GX I/O Input Delay for Row Pins (Part 1 of 3)

| I/O Standard | Parameter | Fast Corner Industrial/ Commercial | -3 Speed Grade (2) | -3 Speed Grade (3) | -4 Speed Grade | -5 Speed Grade | Unit |
|--------------|-------------|------------------------------------|--------------------|--------------------|----------------|----------------|------|
| LVTTTL | t_{PI} | 749 | 1287 | 1350 | 1435 | 1723 | ps |
| | t_{PCOUT} | 410 | 760 | 798 | 848 | 1018 | ps |
| 2.5 V | t_{PI} | 761 | 1273 | 1335 | 1419 | 1704 | ps |
| | t_{PCOUT} | 422 | 746 | 783 | 832 | 999 | ps |
| 1.8 V | t_{PI} | 827 | 1427 | 1497 | 1591 | 1911 | ps |
| | t_{PCOUT} | 488 | 900 | 945 | 1004 | 1206 | ps |
| 1.5 V | t_{PI} | 830 | 1498 | 1571 | 1671 | 2006 | ps |
| | t_{PCOUT} | 491 | 971 | 1019 | 1084 | 1301 | ps |

Table 4–85. Stratix II GX I/O Input Delay for Row Pins (Part 2 of 3)

| I/O Standard | Parameter | Fast Corner Industrial/Commercial | -3 Speed Grade (2) | -3 Speed Grade (3) | -4 Speed Grade | -5 Speed Grade | Unit |
|------------------------------|--------------------|-----------------------------------|--------------------|--------------------|----------------|----------------|------|
| LVCMOS | t _{PI} | 749 | 1287 | 1350 | 1435 | 1723 | ps |
| | t _{PCOUT} | 410 | 760 | 798 | 848 | 1018 | ps |
| SSTL-2 Class I | t _{PI} | 573 | 879 | 921 | 980 | 1176 | ps |
| | t _{PCOUT} | 234 | 352 | 369 | 393 | 471 | ps |
| SSTL-2 Class II | t _{PI} | 573 | 879 | 921 | 980 | 1176 | ps |
| | t _{PCOUT} | 234 | 352 | 369 | 393 | 471 | ps |
| SSTL-18 Class I | t _{PI} | 605 | 960 | 1006 | 1070 | 1285 | ps |
| | t _{PCOUT} | 266 | 433 | 454 | 483 | 580 | ps |
| SSTL-18 Class II | t _{PI} | 605 | 960 | 1006 | 1070 | 1285 | ps |
| | t _{PCOUT} | 266 | 433 | 454 | 483 | 580 | ps |
| 1.5-V HSTL Class I | t _{PI} | 631 | 1056 | 1107 | 1177 | 1413 | ps |
| | t _{PCOUT} | 292 | 529 | 555 | 590 | 708 | ps |
| 1.5-V HSTL Class II | t _{PI} | 631 | 1056 | 1107 | 1177 | 1413 | ps |
| | t _{PCOUT} | 292 | 529 | 555 | 590 | 708 | ps |
| 1.8-V HSTL Class I | t _{PI} | 605 | 960 | 1006 | 1070 | 1285 | ps |
| | t _{PCOUT} | 266 | 433 | 454 | 483 | 580 | ps |
| 1.8-V HSTL Class II | t _{PI} | 605 | 960 | 1006 | 1070 | 1285 | ps |
| | t _{PCOUT} | 266 | 433 | 454 | 483 | 580 | ps |
| PCI | t _{PI} | 830 | 1498 | 1571 | 1671 | 2006 | ps |
| | t _{PCOUT} | 491 | 971 | 1019 | 1084 | 1301 | ps |
| PCI-X | t _{PI} | 830 | 1498 | 1571 | 1671 | 2006 | ps |
| | t _{PCOUT} | 491 | 971 | 1019 | 1084 | 1301 | ps |
| LVDS (1) | t _{PI} | 540 | 948 | 994 | 1057 | 1269 | ps |
| | t _{PCOUT} | 201 | 421 | 442 | 470 | 564 | ps |
| HyperTransport | t _{PI} | 540 | 948 | 994 | 1057 | 1269 | ps |
| | t _{PCOUT} | 201 | 421 | 442 | 470 | 564 | ps |
| Differential SSTL-2 Class I | t _{PI} | 573 | 879 | 921 | 980 | 1176 | ps |
| | t _{PCOUT} | 234 | 352 | 369 | 393 | 471 | ps |
| Differential SSTL-2 Class II | t _{PI} | 573 | 879 | 921 | 980 | 1176 | ps |
| | t _{PCOUT} | 234 | 352 | 369 | 393 | 471 | ps |

Table 4–85. Stratix II GX I/O Input Delay for Row Pins (Part 3 of 3)

| I/O Standard | Parameter | Fast Corner Industrial/Commercial | -3 Speed Grade (2) | -3 Speed Grade (3) | -4 Speed Grade | -5 Speed Grade | Unit |
|----------------------------------|-------------|-----------------------------------|--------------------|--------------------|----------------|----------------|------|
| Differential SSTL-18 Class I | t_{PI} | 605 | 960 | 1006 | 1070 | 1285 | ps |
| | t_{PCOUT} | 266 | 433 | 454 | 483 | 580 | ps |
| Differential SSTL-18 Class II | t_{PI} | 605 | 960 | 1006 | 1070 | 1285 | ps |
| | t_{PCOUT} | 266 | 433 | 454 | 483 | 580 | ps |
| 1.8-V differential HSTL Class I | t_{PI} | 605 | 960 | 1006 | 1070 | 1285 | ps |
| | t_{PCOUT} | 266 | 433 | 454 | 483 | 580 | ps |
| 1.8-V differential HSTL Class II | t_{PI} | 605 | 960 | 1006 | 1070 | 1285 | ps |
| | t_{PCOUT} | 266 | 433 | 454 | 483 | 580 | ps |
| 1.5-V differential HSTL Class I | t_{PI} | 631 | 1056 | 1107 | 1177 | 1413 | ps |
| | t_{PCOUT} | 292 | 529 | 555 | 590 | 708 | ps |
| 1.5-V differential HSTL Class II | t_{PI} | 631 | 1056 | 1107 | 1177 | 1413 | ps |
| | t_{PCOUT} | 292 | 529 | 555 | 590 | 708 | ps |

- (1) The parameters are only available on the left side of the device.
- (2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
- (3) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–86. Stratix II GX I/O Output Delay for Column Pins (Part 1 of 7)

| I/O Standard | Drive Strength | Parameter | Fast Corner Industrial/Commercial | -3 Speed Grade (3) | -3 Speed Grade (4) | -4 Speed Grade | -5 Speed Grade | Unit | |
|--------------|----------------|------------------|-----------------------------------|--------------------|--------------------|----------------|----------------|------|----|
| LVTTTL | 4 mA | t _{OP} | 1236 | 2351 | 2467 | 2624 | 2820 | ps | |
| | | t _{DIP} | 1258 | 2417 | 2537 | 2698 | 2910 | ps | |
| | 8 mA | t _{OP} | 1091 | 2036 | 2136 | 2272 | 2448 | ps | |
| | | t _{DIP} | 1113 | 2102 | 2206 | 2346 | 2538 | ps | |
| | 12 mA | t _{OP} | 1024 | 2036 | 2136 | 2272 | 2448 | ps | |
| | | t _{DIP} | 1046 | 2102 | 2206 | 2346 | 2538 | ps | |
| | 16 mA | t _{OP} | 998 | 1893 | 1986 | 2112 | 2279 | ps | |
| | | t _{DIP} | 1020 | 1959 | 2056 | 2186 | 2369 | ps | |
| | 20 mA | t _{OP} | 976 | 1787 | 1875 | 1994 | 2154 | ps | |
| | | t _{DIP} | 998 | 1853 | 1945 | 2068 | 2244 | ps | |
| | 24 mA (1) | t _{OP} | 969 | 1788 | 1876 | 1995 | 2156 | ps | |
| | | t _{DIP} | 991 | 1854 | 1946 | 2069 | 2246 | ps | |
| | LVCMOS | 4 mA | t _{OP} | 1091 | 2036 | 2136 | 2272 | 2448 | ps |
| | | | t _{DIP} | 1113 | 2102 | 2206 | 2346 | 2538 | ps |
| 8 mA | | t _{OP} | 999 | 1786 | 1874 | 1993 | 2153 | ps | |
| | | t _{DIP} | 1021 | 1852 | 1944 | 2067 | 2243 | ps | |
| 12 mA | | t _{OP} | 971 | 1720 | 1805 | 1919 | 2075 | ps | |
| | | t _{DIP} | 993 | 1786 | 1875 | 1993 | 2165 | ps | |
| 16 mA | | t _{OP} | 978 | 1693 | 1776 | 1889 | 2043 | ps | |
| | | t _{DIP} | 1000 | 1759 | 1846 | 1963 | 2133 | ps | |
| 20 mA | | t _{OP} | 965 | 1677 | 1759 | 1871 | 2025 | ps | |
| | | t _{DIP} | 987 | 1743 | 1829 | 1945 | 2115 | ps | |
| 24 mA (1) | | t _{OP} | 954 | 1659 | 1741 | 1851 | 2003 | ps | |
| | | t _{DIP} | 976 | 1725 | 1811 | 1925 | 2093 | ps | |

Table 4–86. Stratix II GX I/O Output Delay for Column Pins (Part 2 of 7)

| I/O Standard | Drive Strength | Parameter | Fast Corner Industrial/Commercial | -3 Speed Grade (3) | -3 Speed Grade (4) | -4 Speed Grade | -5 Speed Grade | Unit |
|--------------|------------------|------------------|-----------------------------------|--------------------|--------------------|----------------|----------------|------|
| 2.5 V | 4 mA | t _{OP} | 1053 | 2063 | 2165 | 2302 | 2480 | ps |
| | | t _{DIP} | 1075 | 2129 | 2235 | 2376 | 2570 | ps |
| | 8 mA | t _{OP} | 1001 | 1841 | 1932 | 2054 | 2218 | ps |
| | | t _{DIP} | 1023 | 1907 | 2002 | 2128 | 2308 | ps |
| | 12 mA | t _{OP} | 980 | 1742 | 1828 | 1944 | 2101 | ps |
| | | t _{DIP} | 1002 | 1808 | 1898 | 2018 | 2191 | ps |
| 16 mA (1) | t _{OP} | 962 | 1679 | 1762 | 1873 | 2027 | ps | |
| | t _{DIP} | 984 | 1745 | 1832 | 1947 | 2117 | ps | |
| 1.8 V | 2 mA | t _{OP} | 1093 | 2904 | 3048 | 3241 | 3472 | ps |
| | | t _{DIP} | 1115 | 2970 | 3118 | 3315 | 3562 | ps |
| | 4 mA | t _{OP} | 1098 | 2248 | 2359 | 2509 | 2698 | ps |
| | | t _{DIP} | 1120 | 2314 | 2429 | 2583 | 2788 | ps |
| | 6 mA | t _{OP} | 1022 | 2024 | 2124 | 2258 | 2434 | ps |
| | | t _{DIP} | 1044 | 2090 | 2194 | 2332 | 2524 | ps |
| | 8 mA | t _{OP} | 1024 | 1947 | 2043 | 2172 | 2343 | ps |
| | | t _{DIP} | 1046 | 2013 | 2113 | 2246 | 2433 | ps |
| | 10 mA | t _{OP} | 978 | 1882 | 1975 | 2100 | 2266 | ps |
| | | t _{DIP} | 1000 | 1948 | 2045 | 2174 | 2356 | ps |
| | 12 mA (1) | t _{OP} | 979 | 1833 | 1923 | 2045 | 2209 | ps |
| | | t _{DIP} | 1001 | 1899 | 1993 | 2119 | 2299 | ps |
| 1.5 V | 2 mA | t _{OP} | 1073 | 2505 | 2629 | 2795 | 3002 | ps |
| | | t _{DIP} | 1095 | 2571 | 2699 | 2869 | 3092 | ps |
| | 4 mA | t _{OP} | 1009 | 2023 | 2123 | 2257 | 2433 | ps |
| | | t _{DIP} | 1031 | 2089 | 2193 | 2331 | 2523 | ps |
| | 6 mA | t _{OP} | 1012 | 1923 | 2018 | 2146 | 2315 | ps |
| | | t _{DIP} | 1034 | 1989 | 2088 | 2220 | 2405 | ps |
| 8 mA (1) | t _{OP} | 971 | 1878 | 1970 | 2095 | 2262 | ps | |
| | t _{DIP} | 993 | 1944 | 2040 | 2169 | 2352 | ps | |

Table 4–86. Stratix II GX I/O Output Delay for Column Pins (Part 3 of 7)

| I/O Standard | Drive Strength | Parameter | Fast Corner Industrial/Commercial | -3 Speed Grade (3) | -3 Speed Grade (4) | -4 Speed Grade | -5 Speed Grade | Unit | |
|-----------------|------------------|------------------|-----------------------------------|--------------------|--------------------|----------------|----------------|------|----|
| SSTL-2 Class I | 8 mA | t _{OP} | 957 | 1715 | 1799 | 1913 | 2041 | ps | |
| | | t _{DIP} | 979 | 1781 | 1869 | 1987 | 2131 | ps | |
| | 12 mA (1) | t _{OP} | 940 | 1672 | 1754 | 1865 | 1991 | ps | |
| | | t _{DIP} | 962 | 1738 | 1824 | 1939 | 2081 | ps | |
| SSTL-2 Class II | 16 mA | t _{OP} | 918 | 1609 | 1688 | 1795 | 1918 | ps | |
| | | t _{DIP} | 940 | 1675 | 1758 | 1869 | 2008 | ps | |
| | 20 mA | t _{OP} | 919 | 1598 | 1676 | 1783 | 1905 | ps | |
| | | t _{DIP} | 941 | 1664 | 1746 | 1857 | 1995 | ps | |
| | 24 mA (1) | t _{OP} | 915 | 1596 | 1674 | 1781 | 1903 | ps | |
| | | t _{DIP} | 937 | 1662 | 1744 | 1855 | 1993 | ps | |
| SSTL-18 Class I | 4 mA | t _{OP} | 953 | 1690 | 1773 | 1886 | 2012 | ps | |
| | | t _{DIP} | 975 | 1756 | 1843 | 1960 | 2102 | ps | |
| | 6 mA | t _{OP} | 958 | 1656 | 1737 | 1848 | 1973 | ps | |
| | | t _{DIP} | 980 | 1722 | 1807 | 1922 | 2063 | ps | |
| | 8 mA | t _{OP} | 937 | 1640 | 1721 | 1830 | 1954 | ps | |
| | | t _{DIP} | 959 | 1706 | 1791 | 1904 | 2044 | ps | |
| | 10 mA | t _{OP} | 942 | 1638 | 1718 | 1827 | 1952 | ps | |
| | | t _{DIP} | 964 | 1704 | 1788 | 1901 | 2042 | ps | |
| | 12 mA (1) | t _{OP} | 936 | 1626 | 1706 | 1814 | 1938 | ps | |
| | | t _{DIP} | 958 | 1692 | 1776 | 1888 | 2028 | ps | |
| | SSTL-18 Class II | 8 mA | t _{OP} | 925 | 1597 | 1675 | 1782 | 1904 | ps |
| | | | t _{DIP} | 947 | 1663 | 1745 | 1856 | 1994 | ps |
| 16 mA | | t _{OP} | 937 | 1578 | 1655 | 1761 | 1882 | ps | |
| | | t _{DIP} | 959 | 1644 | 1725 | 1835 | 1972 | ps | |
| 18 mA | | t _{OP} | 933 | 1585 | 1663 | 1768 | 1890 | ps | |
| | | t _{DIP} | 955 | 1651 | 1733 | 1842 | 1980 | ps | |
| 20 mA (1) | | t _{OP} | 933 | 1583 | 1661 | 1766 | 1888 | ps | |
| | | t _{DIP} | 955 | 1649 | 1731 | 1840 | 1978 | ps | |

Table 4–86. Stratix II GX I/O Output Delay for Column Pins (Part 4 of 7)

| I/O Standard | Drive Strength | Parameter | Fast Corner Industrial/Commercial | -3 Speed Grade (3) | -3 Speed Grade (4) | -4 Speed Grade | -5 Speed Grade | Unit | |
|--------------------|---------------------|------------------|-----------------------------------|--------------------|--------------------|----------------|----------------|------|----|
| 1.8-V HSTL Class I | 4 mA | t _{OP} | 956 | 1608 | 1687 | 1794 | 1943 | ps | |
| | | t _{DIP} | 978 | 1674 | 1757 | 1868 | 2033 | ps | |
| | 6 mA | t _{OP} | 962 | 1595 | 1673 | 1779 | 1928 | ps | |
| | | t _{DIP} | 984 | 1661 | 1743 | 1853 | 2018 | ps | |
| | 8 mA | t _{OP} | 940 | 1586 | 1664 | 1769 | 1917 | ps | |
| | | t _{DIP} | 962 | 1652 | 1734 | 1843 | 2007 | ps | |
| | 10 mA | t _{OP} | 944 | 1591 | 1669 | 1775 | 1923 | ps | |
| | | t _{DIP} | 966 | 1657 | 1739 | 1849 | 2013 | ps | |
| | 12 mA (1) | t _{OP} | 936 | 1585 | 1663 | 1768 | 1916 | ps | |
| | | t _{DIP} | 958 | 1651 | 1733 | 1842 | 2006 | ps | |
| | 1.8-V HSTL Class II | 16 mA | t _{OP} | 919 | 1385 | 1453 | 1545 | 1680 | ps |
| | | | t _{DIP} | 941 | 1451 | 1523 | 1619 | 1770 | ps |
| 18 mA | | t _{OP} | 921 | 1394 | 1462 | 1555 | 1691 | ps | |
| | | t _{DIP} | 943 | 1460 | 1532 | 1629 | 1781 | ps | |
| 20 mA (1) | | t _{OP} | 921 | 1402 | 1471 | 1564 | 1700 | ps | |
| | | t _{DIP} | 943 | 1468 | 1541 | 1638 | 1790 | ps | |
| 1.5-V HSTL Class I | 4 mA | t _{OP} | 956 | 1607 | 1686 | 1793 | 1942 | ps | |
| | | t _{DIP} | 978 | 1673 | 1756 | 1867 | 2032 | ps | |
| | 6 mA | t _{OP} | 961 | 1588 | 1666 | 1772 | 1920 | ps | |
| | | t _{DIP} | 983 | 1654 | 1736 | 1846 | 2010 | ps | |
| | 8 mA | t _{OP} | 943 | 1590 | 1668 | 1774 | 1922 | ps | |
| | | t _{DIP} | 965 | 1656 | 1738 | 1848 | 2012 | ps | |
| | 10 mA | t _{OP} | 943 | 1592 | 1670 | 1776 | 1924 | ps | |
| | | t _{DIP} | 965 | 1658 | 1740 | 1850 | 2014 | ps | |
| | 12 mA (1) | t _{OP} | 937 | 1590 | 1668 | 1774 | 1922 | ps | |
| | | t _{DIP} | 959 | 1656 | 1738 | 1848 | 2012 | ps | |

Table 4–86. Stratix II GX I/O Output Delay for Column Pins (Part 5 of 7)

| I/O Standard | Drive Strength | Parameter | Fast Corner Industrial/Commercial | -3 Speed Grade (3) | -3 Speed Grade (4) | -4 Speed Grade | -5 Speed Grade | Unit |
|----------------------------------|----------------|------------------|-----------------------------------|--------------------|--------------------|----------------|----------------|------|
| 1.5-V HSTL Class II | 16 mA | t _{OP} | 924 | 1431 | 1501 | 1596 | 1734 | ps |
| | | t _{DIP} | 946 | 1497 | 1571 | 1670 | 1824 | ps |
| | 18 mA | t _{OP} | 927 | 1439 | 1510 | 1605 | 1744 | ps |
| | | t _{DIP} | 949 | 1505 | 1580 | 1679 | 1834 | ps |
| | 20 mA (1) | t _{OP} | 929 | 1450 | 1521 | 1618 | 1757 | ps |
| | | t _{DIP} | 951 | 1516 | 1591 | 1692 | 1847 | ps |
| PCI | - | t _{OP} | 1082 | 1956 | 2051 | 2176 | 2070 | ps |
| | | t _{DIP} | 1104 | 2022 | 2121 | 2250 | 2160 | ps |
| PCI-X | - | t _{OP} | 1082 | 1956 | 2051 | 2176 | 2070 | ps |
| | | t _{DIP} | 1104 | 2022 | 2121 | 2250 | 2160 | ps |
| Differential SSTL-2 Class I (2) | 8 mA | t _{OP} | 957 | 1715 | 1799 | 1913 | 2041 | ps |
| | | t _{DIP} | 979 | 1781 | 1869 | 1987 | 2131 | ps |
| | 12 mA | t _{OP} | 940 | 1672 | 1754 | 1865 | 1991 | ps |
| | | t _{DIP} | 962 | 1738 | 1824 | 1939 | 2081 | ps |
| Differential SSTL-2 Class II (2) | 16 mA | t _{OP} | 918 | 1609 | 1688 | 1795 | 1918 | ps |
| | | t _{DIP} | 940 | 1675 | 1758 | 1869 | 2008 | ps |
| | 20 mA | t _{OP} | 919 | 1598 | 1676 | 1783 | 1905 | ps |
| | | t _{DIP} | 941 | 1664 | 1746 | 1857 | 1995 | ps |
| | 24 mA | t _{OP} | 915 | 1596 | 1674 | 1781 | 1903 | ps |
| | | t _{DIP} | 937 | 1662 | 1744 | 1855 | 1993 | ps |
| Differential SSTL-18 Class I (2) | 4 mA | t _{OP} | 953 | 1690 | 1773 | 1886 | 2012 | ps |
| | | t _{DIP} | 975 | 1756 | 1843 | 1960 | 2102 | ps |
| | 6 mA | t _{OP} | 958 | 1656 | 1737 | 1848 | 1973 | ps |
| | | t _{DIP} | 980 | 1722 | 1807 | 1922 | 2063 | ps |
| | 8 mA | t _{OP} | 937 | 1640 | 1721 | 1830 | 1954 | ps |
| | | t _{DIP} | 959 | 1706 | 1791 | 1904 | 2044 | ps |
| | 10 mA | t _{OP} | 942 | 1638 | 1718 | 1827 | 1952 | ps |
| | | t _{DIP} | 964 | 1704 | 1788 | 1901 | 2042 | ps |
| | 12 mA | t _{OP} | 936 | 1626 | 1706 | 1814 | 1938 | ps |
| | | t _{DIP} | 958 | 1692 | 1776 | 1888 | 2028 | ps |

Table 4–86. Stratix II GX I/O Output Delay for Column Pins (Part 6 of 7)

| I/O Standard | Drive Strength | Parameter | Fast Corner Industrial/ Commercial | -3 Speed Grade (3) | -3 Speed Grade (4) | -4 Speed Grade | -5 Speed Grade | Unit |
|--------------------------------------|----------------|------------------|------------------------------------|--------------------|--------------------|----------------|----------------|------|
| Differential SSTL-18 Class II (2) | 8 mA | t _{OP} | 925 | 1597 | 1675 | 1782 | 1904 | ps |
| | | t _{DIP} | 947 | 1663 | 1745 | 1856 | 1994 | ps |
| | 16 mA | t _{OP} | 937 | 1578 | 1655 | 1761 | 1882 | ps |
| | | t _{DIP} | 959 | 1644 | 1725 | 1835 | 1972 | ps |
| | 18 mA | t _{OP} | 933 | 1585 | 1663 | 1768 | 1890 | ps |
| | | t _{DIP} | 955 | 1651 | 1733 | 1842 | 1980 | ps |
| | 20 mA | t _{OP} | 933 | 1583 | 1661 | 1766 | 1888 | ps |
| | | t _{DIP} | 955 | 1649 | 1731 | 1840 | 1978 | ps |
| 1.8-V differential HSTL Class I (2) | 4 mA | t _{OP} | 956 | 1608 | 1687 | 1794 | 1943 | ps |
| | | t _{DIP} | 978 | 1674 | 1757 | 1868 | 2033 | ps |
| | 6 mA | t _{OP} | 962 | 1595 | 1673 | 1779 | 1928 | ps |
| | | t _{DIP} | 984 | 1661 | 1743 | 1853 | 2018 | ps |
| | 8 mA | t _{OP} | 940 | 1586 | 1664 | 1769 | 1917 | ps |
| | | t _{DIP} | 962 | 1652 | 1734 | 1843 | 2007 | ps |
| | 10 mA | t _{OP} | 944 | 1591 | 1669 | 1775 | 1923 | ps |
| | | t _{DIP} | 966 | 1657 | 1739 | 1849 | 2013 | ps |
| | 12 mA | t _{OP} | 936 | 1585 | 1663 | 1768 | 1916 | ps |
| | | t _{DIP} | 958 | 1651 | 1733 | 1842 | 2006 | ps |
| 1.8-V differential HSTL Class II (2) | 16 mA | t _{OP} | 919 | 1385 | 1453 | 1545 | 1680 | ps |
| | | t _{DIP} | 941 | 1451 | 1523 | 1619 | 1770 | ps |
| | 18 mA | t _{OP} | 921 | 1394 | 1462 | 1555 | 1691 | ps |
| | | t _{DIP} | 943 | 1460 | 1532 | 1629 | 1781 | ps |
| | 20 mA | t _{OP} | 921 | 1402 | 1471 | 1564 | 1700 | ps |
| t _{DIP} | | 943 | 1468 | 1541 | 1638 | 1790 | ps | |

Table 4–86. Stratix II GX I/O Output Delay for Column Pins (Part 7 of 7)

| I/O Standard | Drive Strength | Parameter | Fast Corner Industrial/Commercial | -3 Speed Grade (3) | -3 Speed Grade (4) | -4 Speed Grade | -5 Speed Grade | Unit | |
|-------------------------------------|--------------------------------------|------------------|-----------------------------------|--------------------|--------------------|----------------|----------------|------|----|
| 1.5-V differential HSTL Class I (2) | 4 mA | t _{OP} | 956 | 1607 | 1686 | 1793 | 1942 | ps | |
| | | t _{DIP} | 978 | 1673 | 1756 | 1867 | 2032 | ps | |
| | 6 mA | t _{OP} | 961 | 1588 | 1666 | 1772 | 1920 | ps | |
| | | t _{DIP} | 983 | 1654 | 1736 | 1846 | 2010 | ps | |
| | 8 mA | t _{OP} | 943 | 1590 | 1668 | 1774 | 1922 | ps | |
| | | t _{DIP} | 965 | 1656 | 1738 | 1848 | 2012 | ps | |
| | 10 mA | t _{OP} | 943 | 1592 | 1670 | 1776 | 1924 | ps | |
| | | t _{DIP} | 965 | 1658 | 1740 | 1850 | 2014 | ps | |
| | 12 mA | t _{OP} | 937 | 1590 | 1668 | 1774 | 1922 | ps | |
| | | t _{DIP} | 959 | 1656 | 1738 | 1848 | 2012 | ps | |
| | 1.5-V differential HSTL Class II (2) | 16 mA | t _{OP} | 924 | 1431 | 1501 | 1596 | 1734 | ps |
| | | | t _{DIP} | 946 | 1497 | 1571 | 1670 | 1824 | ps |
| 18 mA | | t _{OP} | 927 | 1439 | 1510 | 1605 | 1744 | ps | |
| | | t _{DIP} | 949 | 1505 | 1580 | 1679 | 1834 | ps | |
| 20 mA | | t _{OP} | 929 | 1450 | 1521 | 1618 | 1757 | ps | |
| | | t _{DIP} | 951 | 1516 | 1591 | 1692 | 1847 | ps | |

- (1) This is the default setting in the Quartus II software.
- (2) These I/O standards are only supported on DQS pins.
- (3) This column refers to -3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
- (4) This column refers to -3 speed grades for EP2SGX130 devices.

Table 4–87. Stratix II GX I/O Output Delay for Row Pins (Part 1 of 4)

| I/O Standard | Drive Strength | Parameter | Fast Corner Industrial/Commercial | -3 Speed Grade (3) | -3 Speed Grade (4) | -4 Speed Grade | -5 Speed Grade | Unit |
|--------------|----------------|------------------|-----------------------------------|--------------------|--------------------|----------------|----------------|------|
| LVTTTL | 4 mA | t _{OP} | 1328 | 2655 | 2786 | 2962 | 3189 | ps |
| | | t _{DIP} | 1285 | 2600 | 2729 | 2902 | 3116 | ps |
| | 8 mA | t _{OP} | 1200 | 2113 | 2217 | 2357 | 2549 | ps |
| | | t _{DIP} | 1157 | 2058 | 2160 | 2297 | 2476 | ps |
| | 12 mA (1) | t _{OP} | 1144 | 2081 | 2184 | 2321 | 2512 | ps |
| | | t _{DIP} | 1101 | 2026 | 2127 | 2261 | 2439 | ps |

Table 4–87. Stratix II GX I/O Output Delay for Row Pins (Part 2 of 4)

| I/O Standard | Drive Strength | Parameter | Fast Corner Industrial/ Commercial | -3 Speed Grade (3) | -3 Speed Grade (4) | -4 Speed Grade | -5 Speed Grade | Unit | |
|-----------------|----------------|------------------|------------------------------------|--------------------|--------------------|----------------|----------------|------|----|
| LVCMOS | 4 mA | t _{OP} | 1200 | 2113 | 2217 | 2357 | 2549 | ps | |
| | | t _{DIP} | 1157 | 2058 | 2160 | 2297 | 2476 | ps | |
| | 8 mA (1) | t _{OP} | 1094 | 1853 | 1944 | 2067 | 2243 | ps | |
| | | t _{DIP} | 1051 | 1798 | 1887 | 2007 | 2170 | ps | |
| | 12 mA (1) | t _{OP} | 1061 | 1723 | 1808 | 1922 | 2089 | ps | |
| | | t _{DIP} | 1018 | 1668 | 1751 | 1862 | 2016 | ps | |
| 2.5 V | 4 mA | t _{OP} | 1183 | 2091 | 2194 | 2332 | 2523 | ps | |
| | | t _{DIP} | 1140 | 2036 | 2137 | 2272 | 2450 | ps | |
| | 8 mA | t _{OP} | 1080 | 1872 | 1964 | 2088 | 2265 | ps | |
| | | t _{DIP} | 1037 | 1817 | 1907 | 2028 | 2192 | ps | |
| | 12 mA (1) | t _{OP} | 1061 | 1775 | 1862 | 1980 | 2151 | ps | |
| | | t _{DIP} | 1018 | 1720 | 1805 | 1920 | 2078 | ps | |
| 1.8 V | 2 mA | t _{OP} | 1253 | 2954 | 3100 | 3296 | 3542 | ps | |
| | | t _{DIP} | 1210 | 2899 | 3043 | 3236 | 3469 | ps | |
| | 4 mA | t _{OP} | 1242 | 2294 | 2407 | 2559 | 2763 | ps | |
| | | t _{DIP} | 1199 | 2239 | 2350 | 2499 | 2690 | ps | |
| | 6 mA | t _{OP} | 1131 | 2039 | 2140 | 2274 | 2462 | ps | |
| | | t _{DIP} | 1088 | 1984 | 2083 | 2214 | 2389 | ps | |
| | 8 mA (1) | t _{OP} | 1100 | 1942 | 2038 | 2166 | 2348 | ps | |
| | | t _{DIP} | 1057 | 1887 | 1981 | 2106 | 2275 | ps | |
| | 1.5 V | 2 mA | t _{OP} | 1213 | 2530 | 2655 | 2823 | 3041 | ps |
| | | | t _{DIP} | 1170 | 2475 | 2598 | 2763 | 2968 | ps |
| 4 mA (1) | | t _{OP} | 1106 | 2020 | 2120 | 2253 | 2440 | ps | |
| | | t _{DIP} | 1063 | 1965 | 2063 | 2193 | 2367 | ps | |
| SSTL-2 Class I | 8 mA | t _{OP} | 1050 | 1759 | 1846 | 1962 | 2104 | ps | |
| | | t _{DIP} | 1007 | 1704 | 1789 | 1902 | 2031 | ps | |
| | 12 mA (1) | t _{OP} | 1026 | 1694 | 1777 | 1889 | 2028 | ps | |
| | | t _{DIP} | 983 | 1639 | 1720 | 1829 | 1955 | ps | |
| SSTL-2 Class II | 16 mA (1) | t _{OP} | 992 | 1581 | 1659 | 1763 | 1897 | ps | |
| | | t _{DIP} | 949 | 1526 | 1602 | 1703 | 1824 | ps | |

Table 4–87. Stratix II GX I/O Output Delay for Row Pins (Part 3 of 4)

| I/O Standard | Drive Strength | Parameter | Fast Corner Industrial/Commercial | -3 Speed Grade (3) | -3 Speed Grade (4) | -4 Speed Grade | -5 Speed Grade | Unit |
|------------------------------|------------------|------------------|-----------------------------------|--------------------|--------------------|----------------|----------------|------|
| SSTL-18 Class I | 4 mA | t _{OP} | 1038 | 1709 | 1793 | 1906 | 2046 | ps |
| | | t _{DIP} | 995 | 1654 | 1736 | 1846 | 1973 | ps |
| | 6 mA | t _{OP} | 1042 | 1648 | 1729 | 1838 | 1975 | ps |
| | | t _{DIP} | 999 | 1593 | 1672 | 1778 | 1902 | ps |
| | 8 mA | t _{OP} | 1018 | 1633 | 1713 | 1821 | 1958 | ps |
| | | t _{DIP} | 975 | 1578 | 1656 | 1761 | 1885 | ps |
| 10 mA (1) | t _{OP} | 1021 | 1615 | 1694 | 1801 | 1937 | ps | |
| | t _{DIP} | 978 | 1560 | 1637 | 1741 | 1864 | ps | |
| 1.8-V HSTL Class I | 4 mA | t _{OP} | 1019 | 1610 | 1689 | 1795 | 1956 | ps |
| | | t _{DIP} | 976 | 1555 | 1632 | 1735 | 1883 | ps |
| | 6 mA | t _{OP} | 1022 | 1580 | 1658 | 1762 | 1920 | ps |
| | | t _{DIP} | 979 | 1525 | 1601 | 1702 | 1847 | ps |
| | 8 mA | t _{OP} | 1004 | 1576 | 1653 | 1757 | 1916 | ps |
| | | t _{DIP} | 961 | 1521 | 1596 | 1697 | 1843 | ps |
| 10 mA | t _{OP} | 1008 | 1567 | 1644 | 1747 | 1905 | ps | |
| | t _{DIP} | 965 | 1512 | 1587 | 1687 | 1832 | ps | |
| 12 mA (1) | t _{OP} | 999 | 1566 | 1643 | 1746 | 1904 | ps | |
| | t _{DIP} | 956 | 1511 | 1586 | 1686 | 1831 | ps | |
| 1.5-V HSTL Class I | 4 mA | t _{OP} | 1018 | 1591 | 1669 | 1774 | 1933 | ps |
| | | t _{DIP} | 975 | 1536 | 1612 | 1714 | 1860 | ps |
| | 6 mA | t _{OP} | 1021 | 1579 | 1657 | 1761 | 1919 | ps |
| | | t _{DIP} | 978 | 1524 | 1600 | 1701 | 1846 | ps |
| 8 mA (1) | t _{OP} | 1006 | 1572 | 1649 | 1753 | 1911 | ps | |
| | t _{DIP} | 963 | 1517 | 1592 | 1693 | 1838 | ps | |
| Differential SSTL-2 Class I | 8 mA | t _{OP} | 1050 | 1759 | 1846 | 1962 | 2104 | ps |
| | | t _{DIP} | 1007 | 1704 | 1789 | 1902 | 2031 | ps |
| | 12 mA | t _{OP} | 1026 | 1694 | 1777 | 1889 | 2028 | ps |
| | | t _{DIP} | 983 | 1639 | 1720 | 1829 | 1955 | ps |
| Differential SSTL-2 Class II | 16 mA | t _{OP} | 992 | 1581 | 1659 | 1763 | 1897 | ps |
| | | t _{DIP} | 949 | 1526 | 1602 | 1703 | 1824 | ps |

Table 4–87. Stratix II GX I/O Output Delay for Row Pins (Part 4 of 4)

| I/O Standard | Drive Strength | Parameter | Fast Corner Industrial/Commercial | -3 Speed Grade (3) | -3 Speed Grade (4) | -4 Speed Grade | -5 Speed Grade | Unit |
|------------------------------|------------------|------------------|-----------------------------------|--------------------|--------------------|----------------|----------------|------|
| Differential SSTL-18 Class I | 4 mA | t _{OP} | 1038 | 1709 | 1793 | 1906 | 2046 | ps |
| | | t _{DIP} | 995 | 1654 | 1736 | 1846 | 1973 | ps |
| | 6 mA | t _{OP} | 1042 | 1648 | 1729 | 1838 | 1975 | ps |
| | | t _{DIP} | 999 | 1593 | 1672 | 1778 | 1902 | ps |
| | 8 mA | t _{OP} | 1018 | 1633 | 1713 | 1821 | 1958 | ps |
| | | t _{DIP} | 975 | 1578 | 1656 | 1761 | 1885 | ps |
| 10 mA | t _{OP} | 1021 | 1615 | 1694 | 1801 | 1937 | ps | |
| | t _{DIP} | 978 | 1560 | 1637 | 1741 | 1864 | ps | |
| LVDS (2) | - | t _{OP} | 1067 | 1723 | 1808 | 1922 | 2089 | ps |
| | | t _{DIP} | 1024 | 1668 | 1751 | 1862 | 2016 | ps |
| HyperTransport | - | t _{OP} | 1053 | 1723 | 1808 | 1922 | 2089 | ps |
| | | t _{DIP} | 1010 | 1668 | 1751 | 1862 | 2016 | ps |

- (1) This is the default setting in the Quartus II software.
- (2) The parameters are only available on the left side of the device.
- (3) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
- (4) This column refers to –3 speed grades for EP2SGX130 devices.

Maximum Input and Output Clock Toggle Rate

Maximum clock toggle rate is defined as the maximum frequency achievable for a clock type signal at an I/O pin. The I/O pin can be a regular I/O pin or a dedicated clock I/O pin.

The maximum clock toggle rate is different from the maximum data bit rate. If the maximum clock toggle rate on a regular I/O pin is 300 MHz, the maximum data bit rate for dual data rate (DDR) could be potentially as high as 600 Mbps on the same I/O pin.

Tables 4–88 through 4–90 specify the maximum input clock toggle rates. Tables 4–91 through 4–96 specify the maximum output clock toggle rates at 0 pF load. Table 4–97 specifies the derating factors for the output clock toggle rate for a non 0 pF load.

To calculate the output toggle rate for a non 0 pF load, use this formula:

The toggle rate for a non 0 pF load

$$= 1,000 / (1,000 / \text{toggle rate at 0 pF load} + \text{derating factor} \times \text{load value in pF} / 1,000)$$

For example, the output toggle rate at 0 pF load for SSTL-18 Class II 20 mA I/O standard is 550 MHz on a -3 device clock output pin. The derating factor is 94 ps/pF. For a 10 pF load the toggle rate is calculated as:

$$1,000 / (1,000 / 550 + 94 \times 10 / 1,000) = 363 \text{ (MHz)}$$

Table 4-88 shows the maximum input clock toggle rates for Stratix II GX device column pins.

| I/O Standard | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
|------------------------------|-----------------------|-----------------------|-----------------------|-------------|
| LVTTTL | 500 | 500 | 450 | MHz |
| 2.5 V | 500 | 500 | 450 | MHz |
| 1.8 V | 500 | 500 | 450 | MHz |
| 1.5 V | 500 | 500 | 450 | MHz |
| LVC MOS | 500 | 500 | 450 | MHz |
| SSTL-2 Class I | 500 | 500 | 500 | MHz |
| SSTL-2 Class II | 500 | 500 | 500 | MHz |
| SSTL-18 Class I | 500 | 500 | 500 | MHz |
| SSTL-18 Class I I | 500 | 500 | 500 | MHz |
| 1.5-V HSTL Class I | 500 | 500 | 500 | MHz |
| 1.5-V HSTL Class II | 500 | 500 | 500 | MHz |
| 1.8-V HSTL Class I | 500 | 500 | 500 | MHz |
| 1.8-V HSTL Class II | 500 | 500 | 500 | MHz |
| PCI | 500 | 500 | 450 | MHz |
| PCI-X | 500 | 500 | 450 | MHz |
| Differential SSTL-2 Class I | 500 | 500 | 500 | MHz |
| Differential SSTL-2 Class II | 500 | 500 | 500 | MHz |
| Differential SSTL-18 Class I | 500 | 500 | 500 | MHz |

Table 4–88. Stratix II GX Maximum Input Clock Rate for Column I/O Pins (Part 2 of 2)

| I/O Standard | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
|-----------------------------------|----------------|----------------|----------------|------|
| Differential SSTL-18 Class I I | 500 | 500 | 500 | MHz |
| 1.8-V differential HSTL Class I | 500 | 500 | 500 | MHz |
| 1.8-V differential HSTL Class II | 500 | 500 | 500 | MHz |
| 1.5-V differential HSTL Class I | 500 | 500 | 500 | MHz |
| 1.5-V differential HSTL Class I I | 500 | 500 | 500 | MHz |
| 1.2-V HSTL | 280 | 250 | 250 | MHz |
| 1.2-V differential HSTL | 280 | 250 | 250 | MHz |

Table 4–89 shows the maximum input clock toggle rates for Stratix II GX device row pins.

Table 4–89. Stratix II GX Maximum Input Clock Rate for Row I/O Pins (Part 1 of 2)

| I/O Standard | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
|-----------------------------|----------------|----------------|----------------|------|
| LVTTTL | 500 | 500 | 450 | MHz |
| 2.5 V | 500 | 500 | 450 | MHz |
| 1.8 V | 500 | 500 | 450 | MHz |
| 1.5 V | 500 | 500 | 450 | MHz |
| LVC MOS | 500 | 500 | 450 | MHz |
| SSTL-2 Class I | 500 | 500 | 500 | MHz |
| SSTL-2 Class II | 500 | 500 | 500 | MHz |
| SSTL-18 Class I | 500 | 500 | 500 | MHz |
| SSTL-18 Class II | 500 | 500 | 500 | MHz |
| 1.5-V HSTL Class I | 500 | 500 | 500 | MHz |
| 1.5-V HSTL Class II | 500 | 500 | 500 | MHz |
| 1.8-V HSTL Class I | 500 | 500 | 500 | MHz |
| 1.8-V HSTL Class II | 500 | 500 | 500 | MHz |
| PCI | 500 | 500 | 425 | MHz |
| PCI-X | 500 | 500 | 425 | MHz |
| Differential SSTL-2 Class I | 500 | 500 | 500 | MHz |

Table 4–89. Stratix II GX Maximum Input Clock Rate for Row I/O Pins (Part 2 of 2)

| I/O Standard | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
|----------------------------------|----------------|----------------|----------------|------|
| Differential SSTL-2 Class II | 500 | 500 | 500 | MHz |
| Differential SSTL-18 Class I | 500 | 500 | 500 | MHz |
| Differential SSTL-18 Class II | 500 | 500 | 500 | MHz |
| 1.8-V differential HSTL Class I | 500 | 500 | 500 | MHz |
| 1.8-V differential HSTL Class II | 500 | 500 | 500 | MHz |
| 1.5-V differential HSTL Class I | 500 | 500 | 500 | MHz |
| 1.5-V differential HSTL Class II | 500 | 500 | 500 | MHz |
| LVDS (1) | 520 | 520 | 420 | MHz |
| HyperTransport | 520 | 520 | 420 | MHz |

(1) The parameters are only available on the left side of the device.

Table 4–90 shows the maximum input clock toggle rates for Stratix II GX device dedicated clock pins.

Table 4–90. Stratix II GX Maximum Input Clock Rate for Dedicated Clock Pins (Part 1 of 2)

| I/O Standard | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
|---------------------|----------------|----------------|----------------|------|
| LVTTTL | 500 | 500 | 400 | MHz |
| 2.5 V | 500 | 500 | 400 | MHz |
| 1.8 V | 500 | 500 | 400 | MHz |
| 1.5 V | 500 | 500 | 400 | MHz |
| LVC MOS | 500 | 500 | 400 | MHz |
| SSTL-2 Class I | 500 | 500 | 500 | MHz |
| SSTL-2 Class II | 500 | 500 | 500 | MHz |
| SSTL-18 Class I | 500 | 500 | 500 | MHz |
| SSTL-18 Class II | 500 | 500 | 500 | MHz |
| 1.5-V HSTL Class I | 500 | 500 | 500 | MHz |
| 1.5-V HSTL Class II | 500 | 500 | 500 | MHz |
| 1.8-V HSTL Class I | 500 | 500 | 500 | MHz |

Table 4–90. Stratix II GX Maximum Input Clock Rate for Dedicated Clock Pins (Part 2 of 2)

| I/O Standard | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
|----------------------------------|----------------|----------------|----------------|------|
| 1.8-V HSTL Class I | 500 | 500 | 500 | MHz |
| PCI | 500 | 500 | 400 | MHz |
| PCI-X | 500 | 500 | 400 | MHz |
| Differential SSTL-2 Class I | 500 | 500 | 500 | MHz |
| Differential SSTL-2 Class II | 500 | 500 | 500 | MHz |
| Differential SSTL-18 Class I | 500 | 500 | 500 | MHz |
| Differential SSTL-18 Class II | 500 | 500 | 500 | MHz |
| 1.8-V differential HSTL Class I | 500 | 500 | 500 | MHz |
| 1.8-V differential HSTL Class II | 500 | 500 | 500 | MHz |
| 1.5-V differential HSTL Class I | 500 | 500 | 500 | MHz |
| 1.5-V differential HSTL Class II | 500 | 500 | 500 | MHz |
| HyperTransport (1) | 717 | 717 | 640 | MHz |
| | 450 | 450 | 400 | MHz |
| LVPECL (1), (2) | 717 | 717 | 640 | MHz |
| | 450 | 450 | 400 | MHz |
| LVDS (1) | 717 | 717 | 640 | MHz |
| | 450 | 450 | 400 | MHz |

- (1) The first set of numbers refers to the HIO dedicated clock pins. The second set of numbers refers to the VIO dedicated clock pins.
- (2) LVPECL is only supported on column clock pins.

Table 4–91 shows the maximum output clock toggle rates for Stratix II GX device column pins.

| I/O Standard | Drive Strength | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
|---------------------|-----------------------|-----------------------|-----------------------|-----------------------|-------------|
| LVTTTL | 4 mA | 270 | 225 | 210 | MHz |
| | 8 mA | 435 | 355 | 325 | MHz |
| | 12 mA | 580 | 475 | 420 | MHz |
| | 16 mA | 720 | 594 | 520 | MHz |
| | 20 mA | 875 | 700 | 610 | MHz |
| | 24 mA (1) | 1030 | 794 | 670 | MHz |
| LVCMOS | 4 mA | 290 | 250 | 230 | MHz |
| | 8 mA | 565 | 480 | 440 | MHz |
| | 12 mA | 790 | 710 | 670 | MHz |
| | 16 mA | 1020 | 925 | 875 | MHz |
| | 20 mA | 1066 | 985 | 935 | MHz |
| | 24 mA (1) | 1100 | 1040 | 1000 | MHz |
| 2.5 V | 4 mA | 230 | 194 | 180 | MHz |
| | 8 mA | 430 | 380 | 380 | MHz |
| | 12 mA | 630 | 575 | 550 | MHz |
| | 16 mA (1) | 930 | 845 | 820 | MHz |
| 1.8 V | 2 mA | 120 | 109 | 104 | MHz |
| | 4 mA | 285 | 250 | 230 | MHz |
| | 6 mA | 450 | 390 | 360 | MHz |
| | 8 mA | 660 | 570 | 520 | MHz |
| | 10 mA | 905 | 805 | 755 | MHz |
| | 12 mA (1) | 1131 | 1040 | 990 | MHz |
| 1.5 V | 2 mA | 244 | 200 | 180 | MHz |
| | 4 mA | 470 | 370 | 325 | MHz |
| | 6 mA | 550 | 430 | 375 | MHz |
| | 8 mA (1) | 625 | 495 | 420 | MHz |
| SSTL-2 Class I | 8 mA | 400 | 300 | 300 | MHz |
| | 12 mA (1) | 400 | 400 | 350 | MHz |
| SSTL-2 Class II | 16 mA | 350 | 350 | 300 | MHz |
| | 20 mA | 400 | 350 | 350 | MHz |
| | 24 mA (1) | 400 | 400 | 350 | MHz |

Table 4–91. Stratix II GX Maximum Output Clock Rate for Column Pins (Part 2 of 3)

| I/O Standard | Drive Strength | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
|------------------------------|----------------|----------------|----------------|----------------|------|
| SSTL-18 Class I | 4 mA | 200 | 150 | 150 | MHz |
| | 6 mA | 350 | 250 | 200 | MHz |
| | 8 mA | 450 | 300 | 300 | MHz |
| | 10 mA | 500 | 400 | 400 | MHz |
| | 12 mA (1) | 700 | 550 | 400 | MHz |
| SSTL-18 Class II | 8 mA | 200 | 200 | 150 | MHz |
| | 16 mA | 400 | 350 | 350 | MHz |
| | 18 mA | 450 | 400 | 400 | MHz |
| | 20 mA (1) | 550 | 500 | 450 | MHz |
| 1.8-V HSTL Class I | 4 mA | 300 | 300 | 300 | MHz |
| | 6 mA | 500 | 450 | 450 | MHz |
| | 8 mA | 650 | 600 | 600 | MHz |
| | 10 mA | 700 | 650 | 600 | MHz |
| | 12 mA (1) | 700 | 700 | 650 | MHz |
| 1.8-V HSTL Class II | 16 mA | 500 | 500 | 450 | MHz |
| | 18 mA | 550 | 500 | 500 | MHz |
| | 20 mA (1) | 650 | 550 | 550 | MHz |
| 1.5-V HSTL Class I | 4 mA | 350 | 300 | 300 | MHz |
| | 6 mA | 500 | 500 | 450 | MHz |
| | 8 mA | 700 | 650 | 600 | MHz |
| | 10 mA | 700 | 700 | 650 | MHz |
| | 12 mA (1) | 700 | 700 | 700 | MHz |
| 1.5-V HSTL Class II | 16 mA | 600 | 600 | 550 | MHz |
| | 18 mA | 650 | 600 | 600 | MHz |
| | 20 mA (1) | 700 | 650 | 600 | MHz |
| PCI | - | 1000 | 790 | 670 | MHz |
| PCI-X | - | 1000 | 790 | 670 | MHz |
| Differential SSTL-2 Class I | 8 mA | 400 | 300 | 300 | MHz |
| | 12 mA | 400 | 400 | 350 | MHz |
| Differential SSTL-2 Class II | 16 mA | 350 | 350 | 300 | MHz |
| | 20 mA | 400 | 350 | 350 | MHz |
| | 24 mA | 400 | 400 | 350 | MHz |

| I/O Standard | Drive Strength | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
|----------------------------------|-----------------------|-----------------------|-----------------------|-----------------------|-------------|
| Differential SSTL-18 Class I | 4 mA | 200 | 150 | 150 | MHz |
| | 6 mA | 350 | 250 | 200 | MHz |
| | 8 mA | 450 | 300 | 300 | MHz |
| | 10 mA | 500 | 400 | 400 | MHz |
| | 12 mA | 700 | 550 | 400 | MHz |
| Differential SSTL-18 Class II | 8 mA | 200 | 200 | 150 | MHz |
| | 16 mA | 400 | 350 | 350 | MHz |
| | 18 mA | 450 | 400 | 400 | MHz |
| | 20 mA | 550 | 500 | 450 | MHz |
| 1.8-V HSTL differential Class I | 4 mA | 300 | 300 | 300 | MHz |
| | 6 mA | 500 | 450 | 450 | MHz |
| | 8 mA | 650 | 600 | 600 | MHz |
| | 10 mA | 700 | 650 | 600 | MHz |
| | 12 mA | 700 | 700 | 650 | MHz |
| 1.8-V HSTL differential Class II | 16 mA | 500 | 500 | 450 | MHz |
| | 18 mA | 550 | 500 | 500 | MHz |
| | 20 mA | 650 | 550 | 550 | MHz |
| 1.5-V HSTL differential Class I | 4 mA | 350 | 300 | 300 | MHz |
| | 6 mA | 500 | 500 | 450 | MHz |
| | 8 mA | 700 | 650 | 600 | MHz |
| | 10 mA | 700 | 700 | 650 | MHz |
| | 12 mA | 700 | 700 | 700 | MHz |
| 1.5-V HSTL differential Class II | 16 mA | 600 | 600 | 550 | MHz |
| | 18 mA | 650 | 600 | 600 | MHz |
| | 20 mA | 700 | 650 | 600 | MHz |

(1) This is the default setting in the Quartus II software.

Table 4–92 shows the maximum output clock toggle rates for Stratix II GX device row pins.

| I/O Standard | Drive Strength | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
|---------------------|-----------------------|-----------------------|-----------------------|-----------------------|-------------|
| LVTTTL | 4 mA | 270 | 225 | 210 | MHz |
| | 8 mA | 435 | 355 | 325 | MHz |
| | 12 mA (1) | 580 | 475 | 420 | MHz |
| LVCMOS | 4 mA | 290 | 250 | 230 | MHz |
| | 8 mA | 565 | 480 | 440 | MHz |
| | 12 mA (1) | 350 | 350 | 297 | MHz |
| 2.5 V | 4 mA | 230 | 194 | 180 | MHz |
| | 8 mA | 430 | 380 | 380 | MHz |
| | 12 mA (1) | 630 | 575 | 550 | MHz |
| 1.8 V | 2 mA | 120 | 109 | 104 | MHz |
| | 4 mA | 285 | 250 | 230 | MHz |
| | 6 mA | 450 | 390 | 360 | MHz |
| | 8 mA (1) | 660 | 570 | 520 | MHz |
| 1.5 V | 2 mA | 244 | 200 | 180 | MHz |
| | 4 mA (1) | 470 | 370 | 325 | MHz |
| SSTL-2 Class I | 8 mA | 400 | 300 | 300 | MHz |
| | 12 mA (1) | 400 | 400 | 350 | MHz |
| SSTL-2 Class II | 16 mA | 350 | 350 | 300 | MHz |
| | 20 mA (1) | 350 | 350 | 297 | MHz |
| SSTL-18 Class I | 4 mA | 200 | 150 | 150 | MHz |
| | 6 mA | 350 | 250 | 200 | MHz |
| | 8 mA | 450 | 300 | 300 | MHz |
| | 10 mA | 500 | 400 | 400 | MHz |
| | 12 mA (1) | 350 | 350 | 297 | MHz |
| 1.8-V HSTL Class I | 4 mA | 300 | 300 | 300 | MHz |
| | 6 mA | 500 | 450 | 450 | MHz |
| | 8 mA | 650 | 600 | 600 | MHz |
| | 10 mA | 700 | 650 | 600 | MHz |
| | 12 mA (1) | 700 | 700 | 650 | MHz |
| 1.5-V HSTL Class I | 4 mA | 350 | 300 | 300 | MHz |
| | 6 mA | 500 | 500 | 450 | MHz |
| | 8 mA (1) | 700 | 650 | 600 | MHz |

Table 4–92. Stratix II GX Maximum Output Clock Rate for Row Pins (Part 2 of 2)

| I/O Standard | Drive Strength | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
|------------------------------|----------------|----------------|----------------|----------------|------|
| Differential SSTL-2 Class I | 8 mA | 400 | 300 | 300 | MHz |
| | 12 mA | 400 | 400 | 350 | MHz |
| Differential SSTL-2 Class II | 16 mA (1) | 350 | 350 | 300 | MHz |
| Differential SSTL-18 Class I | 4 mA | 200 | 150 | 150 | MHz |
| | 6 mA | 350 | 250 | 200 | MHz |
| | 8 mA | 450 | 300 | 300 | MHz |
| | 10 mA (1) | 500 | 400 | 400 | MHz |
| LVDS | - | 717 | 717 | 640 | MHz |
| HyperTransport | - | 717 | 717 | 640 | MHz |

(1) This is the default setting in Quartus II software.

Table 4–93 shows the maximum output clock toggle rate for Stratix II GX device dedicated clock pins.

Table 4–93. Stratix II GX Maximum Output Clock Rate for Dedicated Clock Pins (Part 1 of 4)

| I/O Standard | Drive Strength | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
|--------------|----------------|----------------|----------------|----------------|------|
| LVTTTL | 4 mA | 270 | 225 | 210 | MHz |
| | 8 mA | 435 | 355 | 325 | MHz |
| | 12 mA | 580 | 475 | 420 | MHz |
| | 16 mA | 720 | 594 | 520 | MHz |
| | 20 mA | 875 | 700 | 610 | MHz |
| | 24 mA (1) | 1030 | 794 | 670 | MHz |
| LVCMOS | 4 mA | 290 | 250 | 230 | MHz |
| | 8 mA | 565 | 480 | 440 | MHz |
| | 12 mA | 790 | 710 | 670 | MHz |
| | 16 mA | 1020 | 925 | 875 | MHz |
| | 20 mA | 1066 | 985 | 935 | MHz |
| | 24 mA (1) | 1100 | 1040 | 1000 | MHz |

Table 4–93. Stratix II GX Maximum Output Clock Rate for Dedicated Clock Pins (Part 2 of 4)

| I/O Standard | Drive Strength | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
|--------------------|----------------|----------------|----------------|----------------|------|
| 2.5 V | 4 mA | 230 | 194 | 180 | MHz |
| | 8 mA | 430 | 380 | 380 | MHz |
| | 12 mA | 630 | 575 | 550 | MHz |
| | 16 mA (1) | 930 | 845 | 820 | MHz |
| 1.8 V | 2 mA | 120 | 109 | 104 | MHz |
| | 4 mA | 285 | 250 | 230 | MHz |
| | 6 mA | 450 | 390 | 360 | MHz |
| | 8 mA | 660 | 570 | 520 | MHz |
| | 10 mA | 905 | 805 | 755 | MHz |
| | 12 mA (1) | 1131 | 1040 | 990 | MHz |
| 1.5 V | 2 mA | 244 | 200 | 180 | MHz |
| | 4 mA | 470 | 370 | 325 | MHz |
| | 6 mA | 550 | 430 | 375 | MHz |
| | 8 mA (1) | 625 | 495 | 420 | MHz |
| SSTL-2 Class I | 8 mA | 400 | 300 | 300 | MHz |
| | 12 mA (1) | 400 | 400 | 350 | MHz |
| SSTL-2 Class II | 16 mA | 350 | 350 | 300 | MHz |
| | 20 mA | 400 | 350 | 350 | MHz |
| | 24 mA (1) | 400 | 400 | 350 | MHz |
| SSTL-18 Class I | 4 mA | 200 | 150 | 150 | MHz |
| | 6 mA | 350 | 250 | 200 | MHz |
| | 8 mA | 450 | 300 | 300 | MHz |
| | 10 mA | 500 | 400 | 400 | MHz |
| | 12 mA (1) | 650 | 550 | 400 | MHz |
| SSTL-18 Class II | 8 mA | 200 | 200 | 150 | MHz |
| | 16 mA | 400 | 350 | 350 | MHz |
| | 18 mA | 450 | 400 | 400 | MHz |
| | 20 mA (1) | 550 | 500 | 450 | MHz |
| 1.8-V HSTL Class I | 4 mA | 300 | 300 | 300 | MHz |
| | 6 mA | 500 | 450 | 450 | MHz |
| | 8 mA | 650 | 600 | 600 | MHz |
| | 10 mA | 700 | 650 | 600 | MHz |
| | 12 mA (1) | 700 | 700 | 650 | MHz |

Table 4–93. Stratix II GX Maximum Output Clock Rate for Dedicated Clock Pins (Part 3 of 4)

| I/O Standard | Drive Strength | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
|-------------------------------|----------------|----------------|----------------|----------------|------|
| 1.8-V HSTL Class II | 16 mA | 500 | 500 | 450 | MHz |
| | 18 mA | 550 | 500 | 500 | MHz |
| | 20 mA (1) | 550 | 550 | 550 | MHz |
| 1.5-V HSTL Class I | 4 mA | 350 | 300 | 300 | MHz |
| | 6 mA | 500 | 500 | 450 | MHz |
| | 8 mA | 700 | 650 | 600 | MHz |
| | 10 mA | 700 | 700 | 650 | MHz |
| | 12 mA (1) | 700 | 700 | 700 | MHz |
| 1.5-V HSTL Class II | 16 mA | 600 | 600 | 550 | MHz |
| | 18 mA | 650 | 600 | 600 | MHz |
| | 20 mA (1) | 700 | 650 | 600 | MHz |
| PCI | - | 1000 | 790 | 670 | MHz |
| PCI-X | - | 1000 | 790 | 670 | MHz |
| Differential SSTL-2 Class I | 8 mA | 400 | 300 | 300 | MHz |
| | 12 mA | 400 | 400 | 350 | MHz |
| Differential SSTL-2 Class II | 16 mA | 350 | 350 | 300 | MHz |
| | 20 mA | 400 | 350 | 350 | MHz |
| | 24 mA | 400 | 400 | 350 | MHz |
| Differential SSTL-18 Class I | 4 mA | 200 | 150 | 150 | MHz |
| | 6 mA | 350 | 250 | 200 | MHz |
| | 8 mA | 450 | 300 | 300 | MHz |
| | 10 mA | 500 | 400 | 400 | MHz |
| | 12 mA | 650 | 550 | 400 | MHz |
| Differential SSTL-18 Class II | 8 mA | 200 | 200 | 150 | MHz |
| | 16 mA | 400 | 350 | 350 | MHz |
| | 18 mA | 450 | 400 | 400 | MHz |
| | 20 mA | 550 | 500 | 450 | MHz |
| 1.8-V differential Class I | 4 mA | 300 | 300 | 300 | MHz |
| | 6 mA | 500 | 450 | 450 | MHz |
| | 8 mA | 650 | 600 | 600 | MHz |
| | 10 mA | 700 | 650 | 600 | MHz |
| | 12 mA | 700 | 700 | 650 | MHz |

Table 4–93. Stratix II GX Maximum Output Clock Rate for Dedicated Clock Pins (Part 4 of 4)

| I/O Standard | Drive Strength | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
|-----------------------------|----------------|----------------|----------------|----------------|------|
| 1.8-V differential Class II | 16 mA | 500 | 500 | 450 | MHz |
| | 18 mA | 550 | 500 | 500 | MHz |
| | 20 mA | 550 | 550 | 550 | MHz |
| 1.5-V differential Class I | 4 mA | 350 | 300 | 300 | MHz |
| | 6 mA | 500 | 500 | 450 | MHz |
| | 8 mA | 700 | 650 | 600 | MHz |
| | 10 mA | 700 | 700 | 650 | MHz |
| | 12 mA | 700 | 700 | 700 | MHz |
| 1.5-V differential Class II | 16 mA | 600 | 600 | 550 | MHz |
| | 18 mA | 650 | 600 | 600 | MHz |
| | 20 mA | 700 | 650 | 600 | MHz |
| HyperTransport | - | 300 | 250 | 125 | MHz |
| LVPECL | - | 450 | 400 | 300 | MHz |

(1) This is the default setting in Quartus II software.

Table 4–94 shows the maximum output clock toggle rate for Stratix II GX device series-terminated column pins.

Table 4–94. Stratix II GX Maximum Output Clock Rate for Column Pins (Series Termination) (Part 1 of 2)

| I/O Standard | Drive Strength | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
|-----------------|----------------|----------------|----------------|----------------|------|
| LVTTTL | OCT_25_OHMS | 400 | 400 | 350 | MHz |
| | OCT_50_OHMS | 400 | 400 | 350 | MHz |
| LVCMOS | OCT_25_OHMS | 350 | 350 | 300 | MHz |
| | OCT_50_OHMS | 350 | 350 | 300 | MHz |
| 2.5 V | OCT_25_OHMS | 350 | 350 | 300 | MHz |
| | OCT_50_OHMS | 350 | 350 | 300 | MHz |
| 1.8 V | OCT_25_OHMS | 700 | 550 | 450 | MHz |
| | OCT_50_OHMS | 700 | 550 | 450 | MHz |
| 1.5 V | OCT_50_OHMS | 550 | 450 | 400 | MHz |
| SSTL-2 Class I | OCT_50_OHMS | 600 | 500 | 500 | MHz |
| SSTL-2 Class II | OCT_25_OHMS | 600 | 550 | 500 | MHz |

| I/O Standard | Drive Strength | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
|----------------------------------|-----------------------|-----------------------|-----------------------|-----------------------|-------------|
| SSTL-18 Class I | OCT_50_OHMS | 560 | 400 | 350 | MHz |
| SSTL-18 Class II | OCT_25_OHMS | 550 | 500 | 450 | MHz |
| 1.5-V HSTL Class I | OCT_50_OHMS | 600 | 550 | 500 | MHz |
| 1.8-V HSTL Class I | OCT_50_OHMS | 650 | 600 | 600 | MHz |
| 1.8-V HSTL Class II | OCT_25_OHMS | 500 | 500 | 450 | MHz |
| Differential SSTL-2 Class I | OCT_50_OHMS | 600 | 500 | 500 | MHz |
| Differential SSTL-2 Class II | OCT_25_OHMS | 600 | 550 | 500 | MHz |
| Differential SSTL-18 Class I | OCT_50_OHMS | 560 | 400 | 350 | MHz |
| Differential SSTL-18 Class II | OCT_25_OHMS | 550 | 500 | 450 | MHz |
| 1.8-V differential HSTL Class I | OCT_50_OHMS | 650 | 600 | 600 | MHz |
| 1.8-V differential HSTL Class II | OCT_25_OHMS | 500 | 500 | 450 | MHz |
| 1.5-V differential HSTL Class I | OCT_50_OHMS | 600 | 550 | 500 | MHz |

Table 4–95 shows the maximum output clock toggle rate for Stratix II GX device series-terminated row pins.

| I/O Standard | Drive Strength | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
|---------------------|-----------------------|-----------------------|-----------------------|-----------------------|-------------|
| LVTTTL | OCT_25_OHMS | 400 | 400 | 350 | MHz |
| | OCT_50_OHMS | 400 | 400 | 350 | MHz |
| LVCMOS | OCT_25_OHMS | 350 | 350 | 300 | MHz |
| | OCT_50_OHMS | 350 | 350 | 300 | MHz |
| 2.5 V | OCT_25_OHMS | 350 | 350 | 300 | MHz |
| | OCT_50_OHMS | 350 | 350 | 300 | MHz |
| 1.8 V | OCT_50_OHMS | 700 | 550 | 450 | MHz |
| 1.5 V | OCT_50_OHMS | 550 | 450 | 400 | MHz |

| I/O Standard | Drive Strength | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
|------------------------------|-----------------------|-----------------------|-----------------------|-----------------------|-------------|
| SSTL-2 Class I | OCT_50_OHMS | 600 | 500 | 500 | MHz |
| SSTL-2 Class II | OCT_25_OHMS | 600 | 550 | 500 | MHz |
| SSTL-18 Class I | OCT_50_OHMS | 590 | 400 | 350 | MHz |
| 1.5-V HSTL Class I | OCT_50_OHMS | 600 | 550 | 500 | MHz |
| 1.8-V HSTL Class I | OCT_50_OHMS | 650 | 600 | 600 | MHz |
| Differential SSTL-2 Class I | OCT_50_OHMS | 600 | 500 | 500 | MHz |
| Differential SSTL-2 Class II | OCT_25_OHMS | 600 | 550 | 500 | MHz |
| Differential SSTL-18 Class I | OCT_50_OHMS | 590 | 400 | 350 | MHz |
| Differential HSTL-18 Class I | OCT_50_OHMS | 650 | 600 | 600 | MHz |
| Differential HSTL-15 Class I | OCT_50_OHMS | 600 | 550 | 500 | |

Table 4–96 shows the maximum output clock toggle rate for Stratix II GX device series-terminated dedicated clock pins.

| I/O Standard | Drive Strength | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
|---------------------|-----------------------|-----------------------|-----------------------|-----------------------|-------------|
| LVTTTL | OCT_25_OHMS | 400 | 400 | 350 | MHz |
| | OCT_50_OHMS | 400 | 400 | 350 | MHz |
| LVCMOS | OCT_25_OHMS | 350 | 350 | 300 | MHz |
| | OCT_50_OHMS | 350 | 350 | 300 | MHz |
| 2.5 V | OCT_25_OHMS | 350 | 350 | 300 | MHz |
| | OCT_50_OHMS | 350 | 350 | 300 | MHz |
| 1.8 V | OCT_25_OHMS | 700 | 550 | 450 | MHz |
| | OCT_50_OHMS | 700 | 550 | 450 | MHz |
| 1.5 V | OCT_50_OHMS | 550 | 450 | 400 | MHz |
| SSTL-2 Class I | OCT_50_OHMS | 600 | 500 | 500 | MHz |
| SSTL-2 Class II | OCT_25_OHMS | 600 | 550 | 500 | MHz |
| SSTL-18 Class I | OCT_50_OHMS | 450 | 400 | 350 | MHz |

Table 4–96. Stratix II GX Maximum Output Clock Rate for Dedicated Clock Pins (Series Termination) (Part 2 of 2)

| I/O Standard | Drive Strength | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
|----------------------------------|----------------|----------------|----------------|----------------|------|
| SSTL-18 Class II | OCT_25_OHMS | 550 | 500 | 450 | MHz |
| 1.5-V HSTL Class I | OCT_50_OHMS | 600 | 550 | 500 | MHz |
| 1.8-V HSTL Class I | OCT_50_OHMS | 650 | 600 | 600 | MHz |
| 1.8-V HSTL Class II | OCT_25_OHMS | 500 | 500 | 450 | MHz |
| Differential SSTL-2 Class I | OCT_50_OHMS | 600 | 500 | 500 | MHz |
| Differential SSTL-2 Class II | OCT_25_OHMS | 600 | 550 | 500 | MHz |
| Differential SSTL-18 Class I | OCT_50_OHMS | 560 | 400 | 350 | MHz |
| Differential SSTL-18 Class II | OCT_25_OHMS | 550 | 500 | 450 | MHz |
| 1.8-V differential HSTL Class I | OCT_50_OHMS | 650 | 600 | 600 | MHz |
| 1.8-V differential HSTL Class II | OCT_25_OHMS | 500 | 500 | 450 | MHz |
| 1.5-V differential HSTL Class I | OCT_50_OHMS | 600 | 550 | 500 | MHz |

Table 4–97 specifies the derating factors for the output clock toggle rate for a non 0 pF load.

Table 4–97. Maximum Output Clock Toggle Rate Derating Factors (Part 1 of 5)

| I/O Standard | Drive Strength | Maximum Output Clock Toggle Rate Derating Factors (ps/pF) | | | | | | | | |
|--------------|----------------|---|-----|-----|--------------|-----|-----|-------------------------|-----|-----|
| | | Column I/O Pins | | | Row I/O Pins | | | Dedicated Clock Outputs | | |
| | | -3 | -4 | -5 | -3 | -4 | -5 | -3 | -4 | -5 |
| 3.3-V LVTTL | 4 mA | 478 | 510 | 510 | 478 | 510 | 510 | 466 | 510 | 510 |
| | 8 mA | 260 | 333 | 333 | 260 | 333 | 333 | 291 | 333 | 333 |
| | 12 mA | 213 | 247 | 247 | 213 | 247 | 247 | 211 | 247 | 247 |
| | 16 mA | 136 | 197 | 197 | - | - | - | 166 | 197 | 197 |
| | 20 mA | 138 | 187 | 187 | - | - | - | 154 | 187 | 187 |
| | 24 mA | 134 | 177 | 177 | - | - | - | 143 | 177 | 177 |

Table 4–97. Maximum Output Clock Toggle Rate Derating Factors (Part 2 of 5)

| I/O Standard | Drive Strength | Maximum Output Clock Toggle Rate Derating Factors (ps/pF) | | | | | | | | |
|-------------------------|----------------|---|-------|-------|--------------|-------|-------|-------------------------|-------|-------|
| | | Column I/O Pins | | | Row I/O Pins | | | Dedicated Clock Outputs | | |
| | | -3 | -4 | -5 | -3 | -4 | -5 | -3 | -4 | -5 |
| 3.3-V LVCMOS | 4 mA | 377 | 391 | 391 | 377 | 391 | 391 | 377 | 391 | 391 |
| | 8 mA | 206 | 212 | 212 | 206 | 212 | 212 | 178 | 212 | 212 |
| | 12 mA | 141 | 145 | 145 | - | - | - | 115 | 145 | 145 |
| | 16 mA | 108 | 111 | 111 | - | - | - | 86 | 111 | 111 |
| | 20 mA | 83 | 88 | 88 | - | - | - | 79 | 88 | 88 |
| | 24 mA | 65 | 72 | 72 | - | - | - | 74 | 72 | 72 |
| 2.5-V LVTTTL/ LVCMOS | 4 mA | 387 | 427 | 427 | 387 | 427 | 427 | 391 | 427 | 427 |
| | 8 mA | 163 | 224 | 224 | 163 | 224 | 224 | 170 | 224 | 224 |
| | 12 mA | 142 | 203 | 203 | 142 | 203 | 203 | 152 | 203 | 203 |
| | 16 mA | 120 | 182 | 182 | - | - | - | 134 | 182 | 182 |
| 1.8-V LVTTTL/ LVCMOS | 2 mA | 951 | 1,421 | 1,421 | 951 | 1,421 | 1,421 | 904 | 1,421 | 1,421 |
| | 4 mA | 405 | 516 | 516 | 405 | 516 | 516 | 393 | 516 | 516 |
| | 6 mA | 261 | 325 | 325 | 261 | 325 | 325 | 253 | 325 | 325 |
| | 8 mA | 223 | 274 | 274 | 223 | 274 | 274 | 224 | 274 | 274 |
| | 10 mA | 194 | 236 | 236 | - | - | - | 199 | 236 | 236 |
| | 12 mA | 174 | 209 | 209 | - | - | - | 180 | 209 | 209 |
| 1.5-V LVTTTL/ LVCMOS | 2 mA | 652 | 963 | 963 | 652 | 963 | 963 | 618 | 963 | 963 |
| | 4 mA | 333 | 347 | 347 | 333 | 347 | 347 | 270 | 347 | 347 |
| | 6 mA | 182 | 247 | 247 | - | - | - | 198 | 247 | 247 |
| | 8 mA | 135 | 194 | 194 | - | - | - | 155 | 194 | 194 |
| SSTL-2 Class I | 8 mA | 364 | 680 | 680 | 364 | 680 | 680 | 350 | 680 | 680 |
| | 12 mA | 163 | 207 | 207 | 163 | 207 | 207 | 188 | 207 | 207 |
| SSTL-2 Class II | 16 mA | 118 | 147 | 147 | 118 | 147 | 147 | 94 | 147 | 147 |
| | 20 mA | 99 | 122 | 122 | - | - | - | 87 | 122 | 122 |
| | 24 mA | 91 | 116 | 116 | - | - | - | 85 | 116 | 116 |
| SSTL-18 Class I | 4 mA | 458 | 570 | 570 | 458 | 570 | 570 | 505 | 570 | 570 |
| | 6 mA | 305 | 380 | 380 | 305 | 380 | 380 | 336 | 380 | 380 |
| | 8 mA | 225 | 282 | 282 | 225 | 282 | 282 | 248 | 282 | 282 |
| | 10 mA | 167 | 220 | 220 | 167 | 220 | 220 | 190 | 220 | 220 |
| | 12 mA | 129 | 175 | 175 | - | - | - | 148 | 175 | 175 |

Table 4–97. Maximum Output Clock Toggle Rate Derating Factors (Part 3 of 5)

| I/O Standard | Drive Strength | Maximum Output Clock Toggle Rate Derating Factors (ps/pF) | | | | | | | | |
|------------------------|----------------|---|-----|-----|--------------|-----|-----|-------------------------|-----|-----|
| | | Column I/O Pins | | | Row I/O Pins | | | Dedicated Clock Outputs | | |
| | | -3 | -4 | -5 | -3 | -4 | -5 | -3 | -4 | -5 |
| SSTL-18 Class II | 8 mA | 173 | 206 | 206 | - | - | - | 155 | 206 | 206 |
| | 16 mA | 150 | 160 | 160 | - | - | - | 140 | 160 | 160 |
| | 18 mA | 120 | 130 | 130 | - | - | - | 110 | 130 | 130 |
| | 20 mA | 109 | 127 | 127 | - | - | - | 94 | 127 | 127 |
| 2.5-V SSTL-2 Class I | 8 mA | 364 | 680 | 680 | 364 | 680 | 680 | 350 | 680 | 680 |
| | 12 mA | 163 | 207 | 207 | 163 | 207 | 207 | 188 | 207 | 207 |
| 2.5-V SSTL-2 Class II | 16 mA | 118 | 147 | 147 | 118 | 147 | 147 | 94 | 147 | 147 |
| | 20 mA | 99 | 122 | 122 | - | - | - | 87 | 122 | 122 |
| | 24 mA | 91 | 116 | 116 | - | - | - | 85 | 116 | 116 |
| 1.8-V SSTL-18 Class I | 4 mA | 458 | 570 | 570 | 458 | 570 | 570 | 505 | 570 | 570 |
| | 6 mA | 305 | 380 | 380 | 305 | 380 | 380 | 336 | 380 | 380 |
| | 8 mA | 225 | 282 | 282 | 225 | 282 | 282 | 248 | 282 | 282 |
| | 10 mA | 167 | 220 | 220 | 167 | 220 | 220 | 190 | 220 | 220 |
| | 12 mA | 129 | 175 | 175 | - | - | - | 148 | 175 | 175 |
| 1.8-V SSTL-18 Class II | 8 mA | 173 | 206 | 206 | - | - | - | 155 | 206 | 206 |
| | 16 mA | 150 | 160 | 160 | - | - | - | 140 | 160 | 160 |
| | 18 mA | 120 | 130 | 130 | - | - | - | 110 | 130 | 130 |
| | 20 mA | 109 | 127 | 127 | - | - | - | 94 | 127 | 127 |
| 1.8-V HSTL Class I | 4 mA | 245 | 282 | 282 | 245 | 282 | 282 | 229 | 282 | 282 |
| | 6 mA | 164 | 188 | 188 | 164 | 188 | 188 | 153 | 188 | 188 |
| | 8 mA | 123 | 140 | 140 | 123 | 140 | 140 | 114 | 140 | 140 |
| | 10 mA | 110 | 124 | 124 | 110 | 124 | 124 | 108 | 124 | 124 |
| | 12 mA | 97 | 110 | 110 | 97 | 110 | 110 | 104 | 110 | 110 |
| 1.8-V HSTL Class II | 16 mA | 101 | 104 | 104 | - | - | - | 99 | 104 | 104 |
| | 18 mA | 98 | 102 | 102 | - | - | - | 93 | 102 | 102 |
| | 20 mA | 93 | 99 | 99 | - | - | - | 88 | 99 | 99 |
| 1.5-V HSTL Class I | 4 mA | 168 | 196 | 196 | 168 | 196 | 196 | 188 | 196 | 196 |
| | 6 mA | 112 | 131 | 131 | 112 | 131 | 131 | 125 | 131 | 131 |
| | 8 mA | 84 | 99 | 99 | 84 | 99 | 99 | 95 | 99 | 99 |
| | 10 mA | 87 | 98 | 98 | - | - | - | 90 | 98 | 98 |
| | 12 mA | 86 | 98 | 98 | - | - | - | 87 | 98 | 98 |

Table 4–97. Maximum Output Clock Toggle Rate Derating Factors (Part 4 of 5)

| I/O Standard | Drive Strength | Maximum Output Clock Toggle Rate Derating Factors (ps/pF) | | | | | | | | |
|--------------------------------------|----------------|---|-----|-----|--------------|----|----|-------------------------|-----|-----|
| | | Column I/O Pins | | | Row I/O Pins | | | Dedicated Clock Outputs | | |
| | | -3 | -4 | -5 | -3 | -4 | -5 | -3 | -4 | -5 |
| 1.5-V HSTL Class II | 16 mA | 95 | 101 | 101 | - | - | - | 96 | 101 | 101 |
| | 18 mA | 95 | 100 | 100 | - | - | - | 101 | 100 | 100 |
| | 20 mA | 94 | 101 | 101 | - | - | - | 104 | 101 | 101 |
| 2.5-V differential SSTL Class II (3) | 8 mA | 364 | 680 | 680 | - | - | - | 350 | 680 | 680 |
| | 12 mA | 163 | 207 | 207 | - | - | - | 188 | 207 | 207 |
| | 16 mA | 118 | 147 | 147 | - | - | - | 94 | 147 | 147 |
| | 20 mA | 99 | 122 | 122 | - | - | - | 87 | 122 | 122 |
| | 24 mA | 91 | 116 | 116 | - | - | - | 85 | 116 | 116 |
| 1.8-V differential SSTL Class I (3) | 4 mA | 458 | 570 | 570 | - | - | - | 505 | 570 | 570 |
| | 6 mA | 305 | 380 | 380 | - | - | - | 336 | 380 | 380 |
| | 8 mA | 225 | 282 | 282 | - | - | - | 248 | 282 | 282 |
| | 10 mA | 167 | 220 | 220 | - | - | - | 190 | 220 | 220 |
| | 12 mA | 129 | 175 | 175 | - | - | - | 148 | 175 | 175 |
| 1.8-V differential SSTL Class II (3) | 8 mA | 173 | 206 | 206 | - | - | - | 155 | 206 | 206 |
| | 16 mA | 150 | 160 | 160 | - | - | - | 140 | 160 | 160 |
| | 18 mA | 120 | 130 | 130 | - | - | - | 110 | 130 | 130 |
| | 20 mA | 109 | 127 | 127 | - | - | - | 94 | 127 | 127 |
| 1.8-V differential HSTL Class I (3) | 4 mA | 245 | 282 | 282 | - | - | - | 229 | 282 | 282 |
| | 6 mA | 164 | 188 | 188 | - | - | - | 153 | 188 | 188 |
| | 8 mA | 123 | 140 | 140 | - | - | - | 114 | 140 | 140 |
| | 10 mA | 110 | 124 | 124 | - | - | - | 108 | 124 | 124 |
| | 12 mA | 97 | 110 | 110 | - | - | - | 104 | 110 | 110 |
| 1.8-V differential HSTL Class II (3) | 16 mA | 101 | 104 | 104 | - | - | - | 99 | 104 | 104 |
| | 18 mA | 98 | 102 | 102 | - | - | - | 93 | 102 | 102 |
| | 20 mA | 93 | 99 | 99 | - | - | - | 88 | 99 | 99 |
| 1.5-V differential HSTL Class I (3) | 4 mA | 168 | 196 | 196 | - | - | - | 188 | 196 | 196 |
| | 6 mA | 112 | 131 | 131 | - | - | - | 125 | 131 | 131 |
| | 8 mA | 84 | 99 | 99 | - | - | - | 95 | 99 | 99 |
| | 10 mA | 87 | 98 | 98 | - | - | - | 90 | 98 | 98 |
| | 12 mA | 86 | 98 | 98 | - | - | - | 87 | 98 | 98 |

Table 4–97. Maximum Output Clock Toggle Rate Derating Factors (Part 5 of 5)

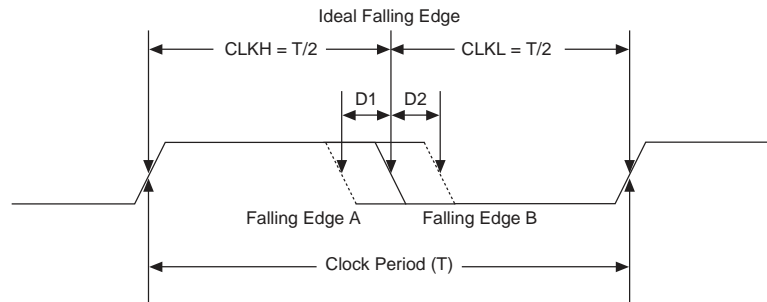
| I/O Standard | Drive Strength | Maximum Output Clock Toggle Rate Derating Factors (ps/pF) | | | | | | | | |
|--------------------------------------|----------------|---|-----|-----|--------------|---------|---------|-------------------------|-----|-----|
| | | Column I/O Pins | | | Row I/O Pins | | | Dedicated Clock Outputs | | |
| | | -3 | -4 | -5 | -3 | -4 | -5 | -3 | -4 | -5 |
| 1.5-V differential HSTL Class II (3) | 16 mA | 95 | 101 | 101 | - | - | - | 96 | 101 | 101 |
| | 18 mA | 95 | 100 | 100 | - | - | - | 101 | 100 | 100 |
| | 20 mA | 94 | 101 | 101 | - | - | - | 104 | 101 | 101 |
| 3.3-V PCI | | 134 | 177 | 177 | - | - | - | 143 | 177 | 177 |
| 3.3-V PCI-X | | 134 | 177 | 177 | - | - | - | 143 | 177 | 177 |
| LVDS | | - | - | - | 155 (1) | 155 (1) | 155 (1) | 134 | 134 | 134 |
| LVPECL (4) | | - | - | - | - | - | - | 134 | 134 | 134 |
| 3.3-V LVTTTL | OCT 50 Ω | 133 | 152 | 152 | 133 | 152 | 152 | 147 | 152 | 152 |
| 2.5-V LVTTTL | OCT 50 Ω | 207 | 274 | 274 | 207 | 274 | 274 | 235 | 274 | 274 |
| 1.8-V LVTTTL | OCT 50 Ω | 151 | 165 | 165 | 151 | 165 | 165 | 153 | 165 | 165 |
| 3.3-V LVCMOS | OCT 50 Ω | 300 | 316 | 316 | 300 | 316 | 316 | 263 | 316 | 316 |
| 1.5-V LVCMOS | OCT 50 Ω | 157 | 171 | 171 | 157 | 171 | 171 | 174 | 171 | 171 |
| SSTL-2 Class I | OCT 50 Ω | 121 | 134 | 134 | 121 | 134 | 134 | 77 | 134 | 134 |
| SSTL-2 Class II | OCT 25 Ω | 56 | 101 | 101 | 56 | 101 | 101 | 58 | 101 | 101 |
| SSTL-18 Class I | OCT 50 Ω | 100 | 123 | 123 | 100 | 123 | 123 | 106 | 123 | 123 |
| SSTL-18 Class II | OCT 25 Ω | 61 | 110 | 110 | - | - | - | 59 | 110 | 110 |
| 1.2-V HSTL (2) | OCT 50 Ω | 95 | - | - | - | - | - | 95 | - | - |

- (1) For LVDS output on row I/O pins the toggle rate derating factors apply to loads larger than 5 pF. In the derating calculation, subtract 5 pF from the intended load value in pF for the correct result. For a load less than or equal to 5 pF, refer to Tables 4–91 through 4–95 for output toggle rates.
- (2) 1.2-V HSTL is only supported on column I/O pins on -3 devices.
- (3) Differential HSTL and SSTL is only supported on column clock and DQS outputs.
- (4) LVPECL is only supported on column clock outputs.

Duty Cycle Distortion

Duty cycle distortion (DCD) describes how much the falling edge of a clock is off from its ideal position. The ideal position is when both the clock high time (CLKH) and the clock low time (CLKL) equal half of the clock period (T), as shown in [Figure 4–11](#). DCD is the deviation of the non-ideal falling edge from the ideal falling edge, such as D1 for the falling edge A and D2 for the falling edge B (see [Figure 4–11](#)). The maximum DCD for a clock is the larger value of D1 and D2.

Figure 4–11. Duty Cycle Distortion



DCD expressed in absolute derivation, for example, D1 or D2 in [Figure 4–11](#), is clock-period independent. DCD can also be expressed as a percentage, and the percentage number is clock-period dependent. DCD as a percentage is defined as:

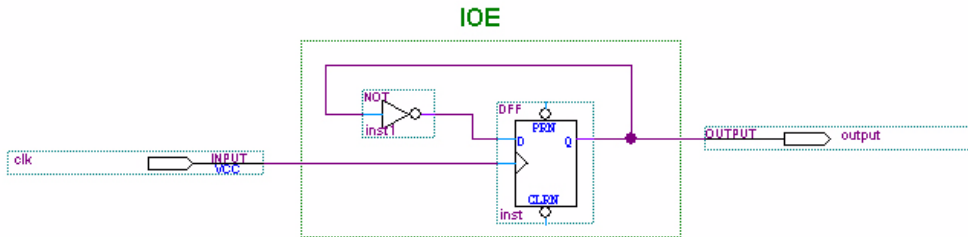
$$(T/2 - D1) / T \text{ (the low percentage boundary)}$$

$$(T/2 + D2) / T \text{ (the high percentage boundary)}$$

DCD Measurement Techniques

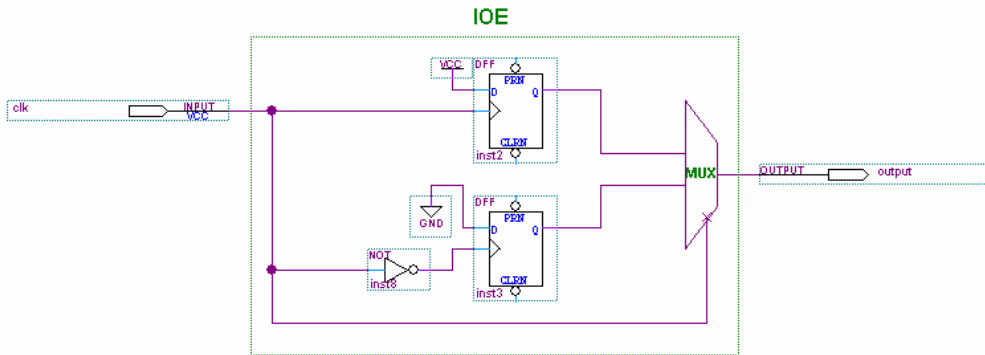
DCD is measured at an FPGA output pin driven by registers inside the corresponding I/O element (IOE) block. When the output is a single data rate signal (non-DDIO), only one edge of the register input clock (positive or negative) triggers output transitions ([Figure 4–12](#)). Therefore, any DCD present on the input clock signal or caused by the clock input buffer or different input I/O standard does not transfer to the output signal.

Figure 4–12. DCD Measurement Technique for Non-DDIO (Single-Data Rate) Outputs



However, when the output is a double data rate input/output (DDIO) signal, both edges of the input clock signal (positive and negative) trigger output transitions (Figure 4–13). Therefore, any distortion on the input clock and the input clock buffer affect the output DCD.

Figure 4–13. DCD Measurement Technique for DDIO (Double-Data Rate) Outputs



When an FPGA PLL generates the internal clock, the PLL output clocks the IOE block. As the PLL only monitors the positive edge of the reference clock input and internally re-creates the output clock signal, any DCD present on the reference clock is filtered out. Therefore, the DCD for a DDIO output with PLL in the clock path is better than the DCD for a DDIO output without PLL in the clock path.

Tables 4–98 through 4–105 show the maximum DCD in absolute derivation for different I/O standards on Stratix II GX devices. Examples are also provided that show how to calculate DCD as a percentage.

| Table 4–98. Maximum DCD for Non-DDIO Output on Row I/O Pins | | | |
|--|---|--------------------------|-------------|
| Row I/O Output Standard | Maximum DCD (ps) for Non-DDIO Output | | |
| | -3 Devices | -4 and -5 Devices | Unit |
| 3.3-V LVTTTL | 245 | 275 | ps |
| 3.3-V LVCMOS | 125 | 155 | ps |
| 2.5 V | 105 | 135 | ps |
| 1.8 V | 180 | 180 | ps |
| 1.5-V LVCMOS | 165 | 195 | ps |
| SSTL-2 Class I | 115 | 145 | ps |
| SSTL-2 Class II | 95 | 125 | ps |
| SSTL-18 Class I | 55 | 85 | ps |
| 1.8-V HSTL Class I | 80 | 100 | ps |
| 1.5-V HSTL Class I | 85 | 115 | ps |
| LVDS | 55 | 80 | ps |

Here is an example for calculating the DCD as a percentage for a non-DDIO output on a row I/O on a -3 device:

If the non-DDIO output I/O standard is SSTL-2 Class II, the maximum DCD is 95 ps (see Table 4–99). If the clock frequency is 267 MHz, the clock period T is:

$$T = 1 / f = 1 / 267 \text{ MHz} = 3.745 \text{ ns} = 3,745 \text{ ps}$$

To calculate the DCD as a percentage:

$$(T/2 - \text{DCD}) / T = (3,745 \text{ ps}/2 - 95 \text{ ps}) / 3,745 \text{ ps} = 47.5\% \text{ (for low boundary)}$$

$$(T/2 + \text{DCD}) / T = (3,745 \text{ ps}/2 + 95 \text{ ps}) / 3,745 \text{ ps} = 52.5\% \text{ (for high boundary)}$$

Therefore, the DCD percentage for the output clock at 267 MHz is from 47.5% to 52.5%.

| Table 4–99. Maximum DCD for Non-DDIO Output on Column I/O Pins | | | |
|---|---|--------------------------|-------------|
| Column I/O Output Standard I/O Standard | Maximum DCD (ps) for Non-DDIO Output | | Unit |
| | -3 Devices | -4 and -5 Devices | |
| 3.3-V LVTTTL | 190 | 220 | ps |
| 3.3-V LVCMOS | 140 | 175 | ps |
| 2.5 V | 125 | 155 | ps |
| 1.8 V | 80 | 110 | ps |
| 1.5-V LVCMOS | 185 | 215 | ps |
| SSTL-2 Class I | 105 | 135 | ps |
| SSTL-2 Class II | 100 | 130 | ps |
| SSTL-18 Class I | 90 | 115 | ps |
| SSTL-18 Class II | 70 | 100 | ps |
| 1.8-V HSTL Class I | 80 | 110 | ps |
| 1.8-V HSTL Class II | 80 | 110 | ps |
| 1.5-V HSTL Class I | 85 | 115 | ps |
| 1.5-V HSTL Class II | 50 | 80 | ps |
| 1.2-V HSTL-12 | 170 | 200 | ps |
| LVPECL | 55 | 80 | ps |

Table 4–100. Maximum DCD for DDIO Output on Row I/O Pins Without PLL in the Clock Path for -3 Devices
Note (1)

| Maximum DCD (ps) for Row DDIO Output I/O Standard | Input I/O Standard (No PLL in Clock Path) | | | | | Unit |
|---|---|---------------|--------|---------------|-------|------|
| | TTL/CMOS | | SSTL-2 | SSTL/HSTL | LVDS | |
| | 3.3 and 2.5 V | 1.8 and 1.5 V | 2.5 V | 1.8 and 1.5 V | 3.3 V | |
| 3.3-V LVTTTL | 260 | 380 | 145 | 145 | 110 | ps |
| 3.3-V LVCMOS | 210 | 330 | 100 | 100 | 65 | ps |
| 2.5 V | 195 | 315 | 85 | 85 | 75 | ps |
| 1.8 V | 150 | 265 | 85 | 85 | 120 | ps |
| 1.5-V LVCMOS | 255 | 370 | 140 | 140 | 105 | ps |
| SSTL-2 Class I | 175 | 295 | 65 | 65 | 70 | ps |
| SSTL-2 Class II | 170 | 290 | 60 | 60 | 75 | ps |
| SSTL-18 Class I | 155 | 275 | 55 | 50 | 90 | ps |
| 1.8-V HSTL Class I | 150 | 270 | 60 | 60 | 95 | ps |
| 1.5-V HSTL Class I | 150 | 270 | 55 | 55 | 90 | ps |
| LVDS | 180 | 180 | 180 | 180 | 180 | ps |

(1) The information in Table 4–100 assumes the input clock has zero DCD.

Here is an example for calculating the DCD in percentage for a DDIO output on a row I/O on a -3 device:

If the input I/O standard is 2.5-V SSTL-2 and the DDIO output I/O standard is SSTL-2 Class= II, the maximum DCD is 60 ps (see Table 4–100). If the clock frequency is 267 MHz, the clock period T is:

$$T = 1 / f = 1 / 267 \text{ MHz} = 3.745 \text{ ns} = 3,745 \text{ ps}$$

Calculate the DCD as a percentage:

$$(T/2 - \text{DCD}) / T = (3,745 \text{ ps}/2 - 60 \text{ ps}) / 3,745 \text{ ps} = 48.4\% \text{ (for low boundary)}$$

$$(T/2 + \text{DCD}) / T = (3,745 \text{ ps}/2 + 60 \text{ ps}) / 3,745 \text{ ps} = 51.6\% \text{ (for high boundary)}$$

Therefore, the DCD percentage for the output clock is from 48.4% to 51.6%.

Table 4–101. Maximum DCD for DDIO Output on Row I/O Pins Without PLL in the Clock Path for -4 and -5 Devices *Note (1)*

| Maximum DCD (ps) for Row DDIO Output I/O Standard | Input I/O Standard (No PLL in the Clock Path) | | | | | Unit |
|---|---|----------|--------|-----------|------|------|
| | TTL/CMOS | | SSTL-2 | SSTL/HSTL | LVDS | |
| | 3.3/2.5V | 1.8/1.5V | 2.5V | 1.8/1.5V | 3.3V | |
| 3.3-V LVTTTL | 440 | 495 | 170 | 160 | 105 | ps |
| 3.3-V LVCMOS | 390 | 450 | 120 | 110 | 75 | ps |
| 2.5 V | 375 | 430 | 105 | 95 | 90 | ps |
| 1.8 V | 325 | 385 | 90 | 100 | 135 | ps |
| 1.5-V LVCMOS | 430 | 490 | 160 | 155 | 100 | ps |
| SSTL-2 Class I | 355 | 410 | 85 | 75 | 85 | ps |
| SSTL-2 Class II | 350 | 405 | 80 | 70 | 90 | ps |
| SSTL-18 Class I | 335 | 390 | 65 | 65 | 105 | ps |
| 1.8-V HSTL Class I | 330 | 385 | 60 | 70 | 110 | ps |
| 1.5-V HSTL Class I | 330 | 390 | 60 | 70 | 105 | ps |
| LVDS | 180 | 180 | 180 | 180 | 180 | ps |

(1) Table 4–101 assumes the input clock has zero DCD.

Table 4–102. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -3 Devices (Part 1 of 2) *Note (1)*

| Maximum DCD (ps) for DDIO Column Output I/O Standard | Input IO Standard (No PLL in the Clock Path) | | | | | Unit |
|--|--|----------|--------|-----------|--------|------|
| | TTL/CMOS | | SSTL-2 | SSTL/HSTL | HSTL12 | |
| | 3.3/2.5V | 1.8/1.5V | 2.5V | 1.8/1.5V | 1.2V | |
| 3.3-V LVTTTL | 260 | 380 | 145 | 145 | 145 | ps |
| 3.3-V LVCMOS | 210 | 330 | 100 | 100 | 100 | ps |
| 2.5 V | 195 | 315 | 85 | 85 | 85 | ps |
| 1.8 V | 150 | 265 | 85 | 85 | 85 | ps |
| 1.5-V LVCMOS | 255 | 370 | 140 | 140 | 140 | ps |
| SSTL-2 Class I | 175 | 295 | 65 | 65 | 65 | ps |
| SSTL-2 Class II | 170 | 290 | 60 | 60 | 60 | ps |
| SSTL-18 Class I | 155 | 275 | 55 | 50 | 50 | ps |

Table 4–102. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -3 Devices (Part 2 of 2) *Note (1)*

| Maximum DCD (ps) for DDIO Column Output I/O Standard | Input IO Standard (No PLL in the Clock Path) | | | | | Unit |
|--|--|----------|--------|-----------|--------|------|
| | TTL/CMOS | | SSTL-2 | SSTL/HSTL | HSTL12 | |
| | 3.3/2.5V | 1.8/1.5V | 2.5V | 1.8/1.5V | 1.2V | |
| SSTL-18 Class II | 140 | 260 | 70 | 70 | 70 | ps |
| 1.8-V HSTL Class I | 150 | 270 | 60 | 60 | 60 | ps |
| 1.8-V HSTL Class II | 150 | 270 | 60 | 60 | 60 | ps |
| 1.5-V HSTL Class I | 150 | 270 | 55 | 55 | 55 | ps |
| 1.5-V HSTL Class II | 125 | 240 | 85 | 85 | 85 | ps |
| 1.2-V HSTL | 240 | 360 | 155 | 155 | 155 | ps |
| LVPECL | 180 | 180 | 180 | 180 | 180 | ps |

(1) Table 4–102 assumes the input clock has zero DCD.

Table 4–103. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -4 and -5 Devices *Note (1)*

| Maximum DCD (ps) for DDIO Column Output I/O Standard | Input IO Standard (No PLL in the Clock Path) | | | | Unit |
|--|--|----------|--------|-----------|------|
| | TTL/CMOS | | SSTL-2 | SSTL/HSTL | |
| | 3.3/2.5V | 1.8/1.5V | 2.5V | 1.8/1.5V | |
| 3.3-V LVTTTL | 440 | 495 | 170 | 160 | ps |
| 3.3-V LVCMOS | 390 | 450 | 120 | 110 | ps |
| 2.5 V | 375 | 430 | 105 | 95 | ps |
| 1.8 V | 325 | 385 | 90 | 100 | ps |
| 1.5-V LVCMOS | 430 | 490 | 160 | 155 | ps |
| SSTL-2 Class I | 355 | 410 | 85 | 75 | ps |
| SSTL-2 Class II | 350 | 405 | 80 | 70 | ps |
| SSTL-18 Class I | 335 | 390 | 65 | 65 | ps |
| SSTL-18 Class II | 320 | 375 | 70 | 80 | ps |
| 1.8-V HSTL Class I | 330 | 385 | 60 | 70 | ps |
| 1.8-V HSTL Class II | 330 | 385 | 60 | 70 | ps |
| 1.5-V HSTL Class I | 330 | 390 | 60 | 70 | ps |
| 1.5-V HSTL Class II | 330 | 360 | 90 | 100 | ps |
| LVPECL | 180 | 180 | 180 | 180 | ps |

(1) Table 4–103 assumes the input clock has zero DCD.

Table 4–104. Maximum DCD for DDIO Output on Row I/O Pins With PLL in the Clock Path

| Maximum DCD (ps) for Row DDIO Output I/O Standard | Stratix II GX Devices (PLL Output Feeding DDIO) | | Unit |
|---|---|------------------|------|
| | -3 Device | -4 and -5 Device | |
| 3.3-V LVTTTL | 110 | 105 | ps |
| 3.3-V LVCMOS | 65 | 75 | ps |
| 2.5V | 75 | 90 | ps |
| 1.8V | 85 | 100 | ps |
| 1.5-V LVCMOS | 105 | 100 | ps |
| SSTL-2 Class I | 65 | 75 | ps |
| SSTL-2 Class II | 60 | 70 | ps |
| SSTL-18 Class I | 50 | 65 | ps |
| 1.8-V HSTL Class I | 50 | 70 | ps |
| 1.5-V HSTL Class I | 55 | 70 | ps |
| LVDS | 180 | 180 | ps |

Table 4–105. Maximum DCD for DDIO Output on Column I/O Pins With PLL in the Clock Path (Part 1 of 2)

| Maximum DCD (ps) for Column DDIO Output I/O Standard | Stratix II GX Devices (PLL Output Feeding DDIO) | | Unit |
|--|---|------------------|------|
| | -3 Device | -4 and -5 Device | |
| 3.3-V LVTTTL | 145 | 160 | ps |
| 3.3-V LVCMOS | 100 | 110 | ps |
| 2.5V | 85 | 95 | ps |
| 1.8V | 85 | 100 | ps |
| 1.5-V LVCMOS | 140 | 155 | ps |
| SSTL-2 Class I | 65 | 75 | ps |
| SSTL-2 Class II | 60 | 70 | ps |
| SSTL-18 Class I | 50 | 65 | ps |
| SSTL-18 Class II | 70 | 80 | ps |
| 1.8-V HSTL Class I | 60 | 70 | ps |
| 1.8-V HSTL Class II | 60 | 70 | ps |
| 1.5-V HSTL Class I | 55 | 70 | ps |
| 1.5-V HSTL Class II | 85 | 100 | ps |

Table 4–105. Maximum DCD for DDIO Output on Column I/O Pins With PLL in the Clock Path (Part 2 of 2)

| Maximum DCD (ps) for Column DDIO Output I/O Standard | Stratix II GX Devices (PLL Output Feeding DDIO) | | Unit |
|--|---|------------------|------|
| | -3 Device | -4 and -5 Device | |
| 1.2-V HSTL | 155 | 155 | ps |
| LVPECL | 180 | 180 | ps |

High-Speed I/O Specifications

Table 4–106 provides high-speed timing specifications definitions.

Table 4–106. High-Speed Timing Specifications and Definitions

| High-Speed Timing Specifications | Definitions |
|----------------------------------|--|
| t_C | High-speed receiver/transmitter input and output clock period. |
| f_{HCLK} | High-speed receiver/transmitter input and output clock frequency. |
| J | Deserialization factor (width of parallel data bus). |
| W | PLL multiplication factor. |
| t_{RISE} | Low-to-high transmission time. |
| t_{FALL} | High-to-low transmission time. |
| Timing unit interval (TUI) | The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = $1/(\text{Receiver Input Clock Frequency} \times \text{Multiplication Factor}) = t_C/w$). |
| f_{IN} | Fast PLL input clock frequency |
| f_{HSDR} | Maximum/minimum LVDS data transfer rate ($f_{HSDR} = 1/TUI$), non-DPA. |
| $f_{HSDRDPA}$ | Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA} = 1/TUI$), DPA. |
| Channel-to-channel skew (TCCS) | The timing difference between the fastest and the slowest output edges including t_{CO} variation and clock skew across channels driven by the same fast PLL. The clock is included in the TCCS measurement. |
| Sampling window (SW) | The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window. |
| Input jitter | Peak-to-peak input jitter on high-speed PLLs. |
| Output jitter | Peak-to-peak output jitter on high-speed PLLs. |
| t_{DUTY} | Duty cycle on high-speed transmitter output clock. |
| t_{LOCK} | Lock time for high-speed transmitter and receiver PLLs. |

Table 4–107 shows the high-speed I/O timing specifications for -3 speed grade Stratix II GX devices.

| Symbol | Conditions | | | -3 Speed Grade | | | Unit | |
|-------------------------------|--|------------|------|----------------|-----|-------|-----------------------|--|
| | | | | Min | Typ | Max | | |
| $f_{IN} = f_{HSDR} / W$ | W = 2 to 32 (LVDS, HyperTransport technology) (3) | | | 16 | | 520 | MHz | |
| | W = 1 (SERDES bypass, LVDS only) | | | 16 | | 500 | MHz | |
| | W = 1 (SERDES used, LVDS only) | | | 150 | | 717 | MHz | |
| f_{HSDR} (data rate) | J = 4 to 10 (LVDS, HyperTransport technology) | | | 150 | | 1,040 | Mbps | |
| | J = 2 (LVDS, HyperTransport technology) | | | (4) | | 760 | Mbps | |
| | J = 1 (LVDS only) | | | (4) | | 500 | Mbps | |
| $f_{HSDRDPA}$ (DPA data rate) | J = 4 to 10 (LVDS, HyperTransport technology) | | | 150 | | 1,040 | Mbps | |
| TCCS | All differential standards | | | - | | 200 | ps | |
| SW | All differential standards | | | 330 | | - | ps | |
| Output jitter | | | | | | 190 | ps | |
| Output t_{RISE} | All differential I/O standards | | | | | 160 | ps | |
| Output t_{FALL} | All differential I/O standards | | | | | 180 | ps | |
| t_{DUTY} | | | | 45 | 50 | 55 | % | |
| DPA run length | | | | | | 6,400 | UI | |
| DPA jitter tolerance (5) | Data channel peak-to-peak jitter | | | 0.44 | | | UI | |
| DPA lock time | | | | | | | Number of repetitions | |
| | SPI-4 | 0000000000 | 10% | 256 | | | | |
| | | 1111111111 | | | | | | |
| | Parallel Rapid I/O | 00001111 | 25% | 256 | | | | |
| | | 10010000 | 50% | 256 | | | | |
| | Miscellaneous | 10101010 | 100% | 256 | | | | |
| 01010101 | | | 256 | | | | | |

- (1) When J = 4 to 10, the SERDES block is used.
- (2) When J = 1 or 2, the SERDES block is bypassed.
- (3) The input clock frequency and the W factor must satisfy the following fast PLL VCO specification: $150 \leq \text{input clock frequency} \times W \leq 1,040$.
- (4) The minimum specification is dependent on the clock source (fast PLL, enhanced PLL, clock pin, and so on) and the clock routing resource (global, regional, or local) utilized. The I/O differential buffer and input register do not have a minimum toggle rate.
- (5) For setup details, refer to the characterization report.

Table 4–108 shows the high-speed I/O timing specifications for -4 speed grade Stratix II GX devices.

| Symbol | Conditions | | | -4 Speed Grade | | | Unit |
|-------------------------------|--|--------------------------|------|----------------|-----|-------|-----------------------|
| | | | | Min | Typ | Max | |
| $f_{IN} = f_{HSDR} / W$ | W = 2 to 32 (LVDS, HyperTransport technology) (3) | | | 16 | | 520 | MHz |
| | W = 1 (SERDES bypass, LVDS only) | | | 16 | | 500 | MHz |
| | W = 1 (SERDES used, LVDS only) | | | 150 | | 717 | MHz |
| f_{HSDR} (data rate) | J = 4 to 10 (LVDS, HyperTransport technology) | | | 150 | | 1,040 | Mbps |
| | J = 2 (LVDS, HyperTransport technology) | | | (4) | | 760 | Mbps |
| | J = 1 (LVDS only) | | | (4) | | 500 | Mbps |
| $f_{HSDRDPA}$ (DPA data rate) | J = 4 to 10 (LVDS, HyperTransport technology) | | | 150 | | 1,040 | Mbps |
| TCCS | All differential standards | | | - | | 200 | ps |
| SW | All differential standards | | | 330 | | - | ps |
| Output jitter | | | | | | 190 | ps |
| Output t_{RISE} | All differential I/O standards | | | | | 160 | ps |
| Output t_{FALL} | All differential I/O standards | | | | | 180 | ps |
| t_{DUTY} | | | | 45 | 50 | 55 | % |
| DPA run length | | | | | | 6,400 | UI |
| DPA jitter tolerance | Data channel peak-to-peak jitter | | | 0.44 | | | UI |
| DPA lock time | | | | | | | Number of repetitions |
| | SPI-4 | 0000000000 1111111111 | 10% | 256 | | | |
| | Parallel Rapid I/O | 00001111 | 25% | 256 | | | |
| | | 10010000 | 50% | 256 | | | |
| | Miscellaneous | 10101010 | 100% | 256 | | | |
| 01010101 | | | 256 | | | | |

- (1) When J = 4 to 10, the SERDES block is used.
- (2) When J = 1 or 2, the SERDES block is bypassed.
- (3) The input clock frequency and the W factor must satisfy the following fast PLL VCO specification: $150 \leq \text{input clock frequency} \times W \leq 1,040$.
- (4) The minimum specification is dependent on the clock source (fast PLL, enhanced PLL, clock pin, and so on) and the clock routing resource (global, regional, or local) utilized. The I/O differential buffer and input register do not have a minimum toggle rate.

Table 4–109 shows the high-speed I/O timing specifications for -5 speed grade Stratix II GX devices.

| Symbol | Conditions | | | -5 Speed Grade | | | Unit |
|-------------------------------|--|------------|-----|----------------|-----|-------|-----------------------|
| | | | | Min | Typ | Max | |
| $f_{IN} = f_{HSDR} / W$ | W = 2 to 32 (LVDS, HyperTransport technology) (3) | | | 16 | | 420 | MHz |
| | W = 1 (SERDES bypass, LVDS only) | | | 16 | | 500 | MHz |
| | W = 1 (SERDES used, LVDS only) | | | 150 | | 640 | MHz |
| f_{HSDR} (data rate) | J = 4 to 10 (LVDS, HyperTransport technology) | | | 150 | | 840 | Mbps |
| | J = 2 (LVDS, HyperTransport technology) | | | (4) | | 700 | Mbps |
| | J = 1 (LVDS only) | | | (4) | | 500 | Mbps |
| $f_{HSDRDPA}$ (DPA data rate) | J = 4 to 10 (LVDS, HyperTransport technology) | | | 150 | | 840 | Mbps |
| TCCS | All differential I/O standards | | | - | | 200 | ps |
| SW | All differential I/O standards | | | 440 | | - | ps |
| Output jitter | | | | | | 190 | ps |
| Output t_{RISE} | All differential I/O standards | | | | | 290 | ps |
| Output t_{FALL} | All differential I/O standards | | | | | 290 | ps |
| t_{DUTY} | | | | 45 | 50 | 55 | % |
| DPA run length | | | | | | 6,400 | UI |
| DPA jitter tolerance | Data channel peak-to-peak jitter | | | 0.44 | | | UI |
| DPA lock time | | | | | | | Number of repetitions |
| | SPI-4 | 0000000000 | 10% | 256 | | | |
| | | 1111111111 | | | | | |
| | Parallel Rapid I/O | 00001111 | 25% | 256 | | | |
| | | 10010000 | 50% | 256 | | | |
| Miscellaneous | 10101010 | 100% | 256 | | | | |
| | 01010101 | | 256 | | | | |

- (1) When J = 4 to 10, the SERDES block is used.
- (2) When J = 1 or 2, the SERDES block is bypassed.
- (3) The input clock frequency and the W factor must satisfy the following fast PLL VCO specification: $150 \leq \text{input clock frequency} \times W \leq 840$.
- (4) The minimum specification is dependent on the clock source (fast PLL, enhanced PLL, clock pin, and so on) and the clock routing resource (global, regional, or local) utilized. The I/O differential buffer and input register do not have a minimum toggle rate.

PLL Timing Specifications

Tables 4–110 and 4–111 describe the Stratix II GX PLL specifications when operating in both the commercial junction temperature range (0 to 85 C) and the industrial junction temperature range (–40 to 100 C), except for the clock switchover and phase-shift stepping features. These two features are only supported from the 0 to 100 C junction temperature range.

Table 4–110. Enhanced PLL Specifications (Part 1 of 2)

| Name | Description | Min | Typ | Max | Unit |
|------------------|--|---------|-------------------|---|-------------------|
| f_{IN} | Input clock frequency | 4 | | 500 | MHz |
| f_{INPFD} | Input frequency to the PFD | 4 | | 420 | MHz |
| f_{INDUTY} | Input clock duty cycle | 40 | | 60 | % |
| f_{ENDUTY} | External feedback input clock duty cycle | 40 | | 60 | % |
| $t_{INJITTER}$ | Input or external feedback clock input jitter tolerance in terms of period jitter. Bandwidth ≤ 0.85 MHz | | 0.5 | | ns (peak-to-peak) |
| | Input or external feedback clock input jitter tolerance in terms of period jitter. Bandwidth > 0.85 MHz | | 1.0 | | ns (peak-to-peak) |
| $t_{OUTJITTER}$ | Dedicated clock output period jitter | | | 250 ps for ≥ 100 MHz outclk 25 mUI for < 100 MHz outclk | ps or mUI (p-p) |
| t_{FCOMP} | External feedback compensation time | | | 10 | ns |
| f_{OUT} | Output frequency for internal global or regional clock | 1.5 (2) | | 550 | MHz |
| $f_{OUTDUTY}$ | Duty cycle for external clock output | 45 | 50 | 55 | % |
| $f_{SCANCLK}$ | Scanclk frequency | | | 100 | MHz |
| $t_{CONFIGEPLL}$ | Time required to reconfigure scan chains for EPLLs | | $174/f_{SCANCLK}$ | | ns |
| f_{OUT_EXT} | PLL external clock output frequency | 1.5 (2) | | (1) | MHz |
| t_{LOCK} | Time required for the PLL to lock from the time it is enabled or the end of device configuration | | 0.03 | 1 | ms |
| t_{DLOCK} | Time required for the PLL to lock dynamically after automatic clock switchover between two identical clock frequencies | | | 1 | ms |
| $f_{SWITCHOVER}$ | Frequency range where the clock switchover performs properly | 1.5 | 1 | 500 | MHz |
| f_{CLBW} | PLL closed-loop bandwidth | 0.13 | 1.2 | 16.9 | MHz |

Table 4–110. Enhanced PLL Specifications (Part 2 of 2)

| Name | Description | Min | Typ | Max | Unit |
|------------------------|--|-----|-----|-------|------|
| f_{VCO} | PLL VCO operating range for –3 and –4 speed grade devices | 300 | | 1,040 | MHz |
| | PLL VCO operating range for –5 speed grade devices | 300 | | 840 | MHz |
| f_{SS} | Spread-spectrum modulation frequency | 100 | | 500 | kHz |
| % spread | Percent down spread for a given clock frequency | 0.4 | 0.5 | 0.6 | % |
| t_{PLL_PSERR} | Accuracy of PLL phase shift | | | ±30 | ps |
| t_{ARESET} | Minimum pulse width on <code>areset</code> signal. | 10 | | | ns |
| $t_{ARESET_RECONFIG}$ | Minimum pulse width on the <code>areset</code> signal when using PLL reconfiguration. Reset the PLL after <code>scandone</code> goes high. | 500 | | | ns |
| $t_{RECONFIGWAIT}$ | The time required for the wait after the reconfiguration is done and the <code>areset</code> is applied. | | | 2 | us |

- (1) This is limited by the I/O f_{MAX} . See Tables 4–91 through 4–95 for the maximum.
- (2) If the counter cascading feature of the PLL is utilized, there is no minimum output clock frequency.

Table 4–111. Fast PLL Specifications (Part 1 of 2)

| Name | Description | Min | Typ | Max | Unit |
|----------------|---|-----|-----|-----|----------|
| f_{IN} | Input clock frequency (for -3 and -4 speed grade devices) | 16 | | 717 | MHz |
| | Input clock frequency (for -5 speed grade devices) | 16 | | 640 | MHz |
| f_{INPFD} | Input frequency to the PFD | 16 | | 500 | MHz |
| f_{INDUTY} | Input clock duty cycle | 40 | | 60 | % |
| $t_{INJITTER}$ | Input clock jitter tolerance in terms of period jitter. Bandwidth \leq MHz | | 0.5 | | ns (p-p) |
| | Input clock jitter tolerance in terms of period jitter. Bandwidth $>$ 0.2 MHz | | 1.0 | | ns (p-p) |

Table 4–111. Fast PLL Specifications (Part 2 of 2)

| Name | Description | Min | Typ | Max | Unit |
|------------------------------|--|--------|-------------------------|-------|------|
| f _{VCO} | Upper VCO frequency range for –3 and –4 speed grades | 300 | | 1,040 | MHz |
| | Upper VCO frequency range for –5 speed grades | 300 | | 840 | MHz |
| | Lower VCO frequency range for –3 and –4 speed grades | 150 | | 520 | MHz |
| | Lower VCO frequency range for –5 speed grades | 150 | | 420 | MHz |
| f _{OUT} | PLL output frequency to GCLK or RCLK | 4.6875 | | 550 | MHz |
| | PLL output frequency to LVDS or DPA clock | 150 | | 1,040 | MHz |
| f _{OUT_EXT} | PLL clock output frequency to regular I/O | 4.6875 | | (1) | MHz |
| t _{CONFIGPLL} | Time required to reconfigure scan chains for fast PLLs | | 75/f _{SCANCLK} | | ns |
| f _{CLBW} | PLL closed-loop bandwidth | 1.16 | 5 | 28 | MHz |
| t _{LOCK} | Time required for the PLL to lock from the time it is enabled or the end of the device configuration | | 0.03 | 1 | ms |
| t _{PLL_PSERR} | Accuracy of PLL phase shift | | | ±30 | ps |
| t _{ARESET} | Minimum pulse width on <i>areset</i> signal. | 10 | | | ns |
| t _{ARESET_RECONFIG} | Minimum pulse width on the <i>areset</i> signal when using PLL reconfiguration. Reset the PLL after <i>scandone</i> goes high. | 500 | | | ns |

(1) This is limited by the I/O f_{MAX}. See Tables 4–91 through 4–95 for the maximum.

External Memory Interface Specifications

Tables 4–112 through 4–116 contain Stratix II GX device specifications for the dedicated circuitry used for interfacing with external memory devices.

Table 4–112. DLL Frequency Range Specifications (Part 1 of 2)

| Frequency Mode | Frequency Range (MHz) | Resolution (Degrees) |
|----------------|------------------------------------|----------------------|
| 0 | 100 to 175 | 30 |
| 1 | 150 to 230 | 22.5 |
| 2 | 200 to 350 (–3 speed grade) | 30 |
| | 200 to 310 (–4 and –5 speed grade) | 30 |

| Table 4–112. DLL Frequency Range Specifications (Part 2 of 2) | | |
|--|------------------------------------|-----------------------------|
| Frequency Mode | Frequency Range (MHz) | Resolution (Degrees) |
| 3 | 240 to 400 (–3 speed grade) | 36 |
| | 240 to 350 (–4 and –5 speed grade) | 36 |

| Table 4–113. DQS Jitter Specifications for DLL-Delayed Clock (t_{DQS_JITTER}) <i>Note (1)</i> | | |
|---|------------------------|------------------------|
| Number of DQS Delay Buffer Stages (2) | Commercial (ps) | Industrial (ps) |
| 1 | 80 | 110 |
| 2 | 110 | 130 |
| 3 | 130 | 180 |
| 4 | 160 | 210 |

- (1) Peak-to-peak period jitter on the phase-shifted DQS clock. For example, jitter on two delay stages under commercial conditions is 200 ps peak-to-peak or 100 ps.
- (2) Delay stages used for requested DQS phase shift are reported in a project's Compilation Report in the Quartus II software.

| Table 4–114. DQS Phase-Shift Error Specifications for DLL-Delayed Clock (t_{DQS_PSERR}) | | | |
|--|----------------------------|----------------------------|----------------------------|
| Number of DQS Delay Buffer Stages (1) | –3 Speed Grade (ps) | –4 Speed Grade (ps) | –5 Speed Grade (ps) |
| 1 | 25 | 30 | 35 |
| 2 | 50 | 60 | 70 |
| 3 | 75 | 90 | 105 |
| 4 | 100 | 120 | 140 |

- (1) Delay stages used for request DQS phase shift are reported in a project's Compilation Report in the Quartus II software. For example, phase-shift error on two delay stages under -3 conditions is 50 ps peak-to-peak or 25 ps.

Table 4–115. DQS Bus Clock Skew Adder Specifications
($t_{bDQS_CLOCK_SKEW_ADDER}$)

| Mode | DQS Clock Skew Adder (ps) (1) |
|---------------|-------------------------------|
| 4 DQ per DQS | 40 |
| 9 DQ per DQS | 70 |
| 18 DQ per DQS | 75 |
| 36 DQ per DQS | 95 |

- (1) This skew specification is the absolute maximum and minimum skew. For example, skew on a 40 DQ group is 40 ps or 20 ps.

Table 4–116. DQS Phase Offset Delay Per Stage (ps) *Notes (1), (2), (3)*

| Speed Grade | Positive Offset | | Negative Offset | |
|-------------|-----------------|-----|-----------------|-----|
| | Min | Max | Min | Max |
| -3 | 10 | 15 | 8 | 11 |
| -4 | 10 | 15 | 8 | 11 |
| -5 | 10 | 16 | 8 | 12 |

- (1) The delay settings are linear.
 (2) The valid settings for phase offset are -32 to +31.
 (3) The typical value equals the average of the minimum and maximum values.

JTAG Timing Specifications

Figure 4–14 shows the timing requirements for the JTAG signals

Figure 4–14. Stratix II GX JTAG Waveforms.

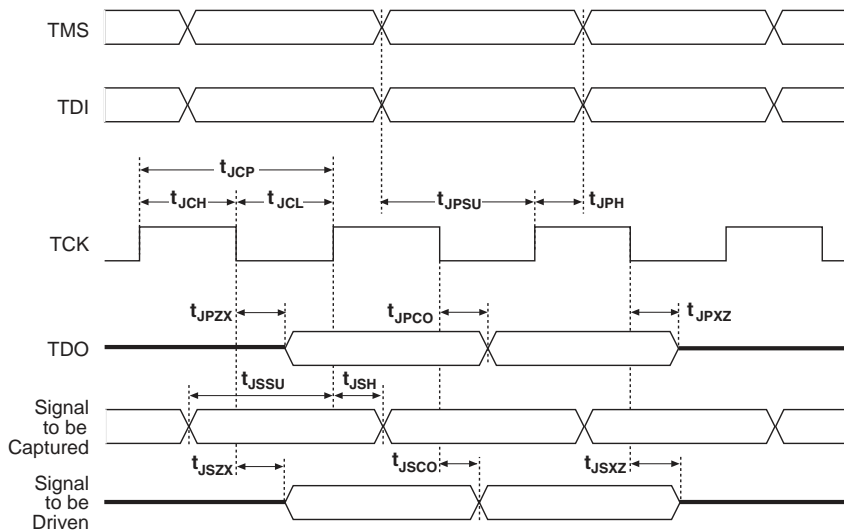


Table 4–117 shows the JTAG timing parameters and values for Stratix II GX devices.

| Symbol | Parameter | Min | Max | Unit |
|------------|--|-----|-----|------|
| t_{JCP} | TCK clock period | 30 | | ns |
| t_{JCH} | TCK clock high time | 12 | | ns |
| t_{JCL} | TCK clock low time | 12 | | ns |
| t_{JPSU} | JTAG port setup time | 4 | | ns |
| t_{JPH} | JTAG port hold time | 5 | | ns |
| t_{JPCO} | JTAG port clock to output | | 9 | ns |
| t_{JPZX} | JTAG port high impedance to valid output | | 9 | ns |
| t_{JPXZ} | JTAG port valid output to high impedance | | 9 | ns |
| t_{JSSU} | Capture register setup time | 4 | | ns |
| t_{JSH} | Capture register hold time | 5 | | ns |
| t_{JSCO} | Update register clock to output | | 12 | ns |
| t_{JSZX} | Update register high impedance to valid output | | 12 | ns |
| t_{JSXZ} | Update register valid output to high impedance | | 12 | ns |

Referenced Documents

This chapter references the following documents:

- *Operating Requirements for Altera Devices Data Sheet*
- *PowerPlay Power Analyzer* chapter in volume 3 of the *Quartus II Handbook*.
- *PowerPlay Early Power Estimator (EPE) and Power Analyzer*
- *Quartus II PowerPlay Analysis and Optimization Technology*
- *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*
- *Stratix II GX Transceiver Architecture Overview* chapter in volume 2 of the *Stratix II GX Device Handbook*
- *Volume 2, Stratix II GX Device Handbook*

Document Revision History

Table 6–105 shows the revision history for this chapter.

| <i>Table 4–118. Document Revision History (Part 1 of 5)</i> | | |
|---|--|---------------------------|
| Date and Document Version | Changes Made | Summary of Changes |
| June 2009 v4.6 | Replaced Table 4–31 Updated: <ul style="list-style-type: none"> ● Table 4–5 ● Table 4–6 ● Table 4–7 ● Table 4–8 ● Table 4–9 ● Table 4–10 ● Table 4–11 ● Table 4–12 ● Table 4–13 ● Table 4–14 ● Table 4–15 ● Table 4–16 ● Table 4–17 ● Table 4–18 ● Table 4–20 ● Table 4–50 ● Table 4–95 ● Table 4–105 ● Table 4–110 ● Table 4–111 | |
| October 2007 v4.5 | Updated: <ul style="list-style-type: none"> ● Table 4–3 ● Table 4–6 ● Table 4–16 ● Table 4–19 ● Table 4–20 ● Table 4–21 ● Table 4–22 ● Table 4–55 ● Table 4–106 ● Table 4–107 ● Table 4–108 ● Table 4–109 ● Table 4–112 | |
| | Updated title only in Tables 4–88 and 4–89. | |
| | Minor text edits. | |

Table 4–118. Document Revision History (Part 2 of 5)

| Date and Document Version | Changes Made | Summary of Changes |
|----------------------------------|--|---------------------------|
| August 2007 v4.4 | Removed note “The data in this table is preliminary. Altera will provide a report upon completion of characterization of the Stratix II GX devices. Conditions for testing the silicon have not been determined.” from each table. | |
| | Removed note “The data in Tables xxx through xxx is preliminary. Altera will provide a report upon completion of characterization of the Stratix II GX devices. Conditions for testing the silicon have not been determined.” in the clock timing parameters sections. | |
| | Updated clock timing parameter Tables 4–63 through 4–78 (Table 4–75 was unchanged). | |
| | Updated Table 4–21 and added new Table 4–22. | |
| | Updated: <ul style="list-style-type: none">● Table 4–6● Table 4–16● Table 4–19● Table 4–49● Table 4–52● Table 4–107 | |
| | Added note to Table 4–50. | |
| | Added: <ul style="list-style-type: none">● Figure 4–3● Figure 4–4● Figure 4–5 | |
| | Added the “Referenced Documents” section. | |
| May 2007 v4.3 | Changed 1.875 KHz to 1.875 MHz in Table 4–19, XAUI Receiver Jitter Tolerance section. | |

Table 4–118. Document Revision History (Part 3 of 5)

| Date and Document Version | Changes Made | Summary of Changes |
|----------------------------------|--|---|
| February 2007 v4.2 | Added the “Document Revision History” section to this chapter. | Added support information for the Stratix II GX device. |
| | Updated Table 4–5: <ul style="list-style-type: none"> ● Removed last three lines ● Removed note 1 ● Added new note 4 | |
| | Deleted table 6-6. | |
| | Replaced Table 4–6 with all new information. | |
| | Added Figures 4–1 and 4–2. | |
| | Added Tables 4–7 through 4–19. | |
| | Removed Figures 6-1 through 6-4. | |
| | Updated Table 4–22: <ul style="list-style-type: none"> ● Changed R_{CONF} information. | |
| | Updated Table 4–52 <ul style="list-style-type: none"> ● SSTL-18 Class I, column 1: changed 25 to 50. | |
| | Updated: <ul style="list-style-type: none"> ● Table 4–54 ● Table 4–87 ● Table 4–91 ● Table 4–94 | |
| | Updated Tables 4–62 through 4–77 | |
| | Updated Tables 4–79 and 4–80 <ul style="list-style-type: none"> ● Added “units” column | |
| | Updated Tables 4–83 through 4–86 <ul style="list-style-type: none"> ● Changed column title to “Fast Corner Industrial/Commercial”. | |
| | Updated Table 4–109. <ul style="list-style-type: none"> ● Added a new line to the bottom of the table. | |
| August 2006 v4.1 | Update Table 6–75, Table 6–84, and Table 6–90. | |

Table 4–118. Document Revision History (Part 4 of 5)

| Date and Document Version | Changes Made | Summary of Changes |
|----------------------------------|--|---|
| June 2006, v4.0 | <ul style="list-style-type: none">● Updated Table 6–5.● Updated Table 6–6.● Updated all values in Table 6–7.● Added Tables 6–8 and 6–9.● Added Figures 6–1 through 6–4.● Updated Table 6–18.● Updated Tables 6–85 through 6–96.● Added Table 6–80, Stratix II GX Maximum Output Clock Rate for Dedicated Clock Pins.● Updated Table 6–100.● In “I/O Timing Measurement Methodology” section, updated Table 6–42.● In “Internal Timing Parameters” section, updated Tables 6–43 through 6–48.● In “Stratix II GX Clock Timing Parameters” section, updated Tables 6–50 through 6–65.● In “IOE Programmable Delay” section, updated Tables 6–67 and 6–68.● In “I/O Delays” section, updated Tables 6–71 through 6–74.● In “Maximum Input & Output Clock Toggle Rate” section, updated Tables 6–75 through 6–83.● In “DCD Measurement Techniques” section, updated Tables 6–85 through 6–92.● In “High-Speed I/O Specifications” section, updated Tables 6–94 through 6–96.● In “External Memory Interface Specifications” section, updated Table 6–100. | <ul style="list-style-type: none">● Removed rows for V_{ID}, V_{OD}, V_{ICM}, and V_{OCM} from Table 6–5.● Updated values for rx, tx, and <code>refclkb</code> in Table 6–6.● Removed table containing 1.2-V PCML I/O information. That information is in Table 6–7.● Added values to Table 6–100. |

Table 4–118. Document Revision History (Part 5 of 5)

| Date and Document Version | Changes Made | Summary of Changes |
|----------------------------------|--|---------------------------|
| April 2006, v3.0 | <ul style="list-style-type: none">● Updated Table 6–3.● Updated Table 6–5.● Updated Table 6–7.● Added Table 6–42.● Updated “Internal Timing Parameters” section (Tables 6–43 through 6–48).● Updated “Stratix II GX Clock Timing Parameters” section (Tables 6–49 through 6–65).● Updated “IOE Programmable Delay” section (Tables 6–67 and 6–68)● Updated “I/O Delays” section (Tables 6–71 through 6–74).● Updated “Maximum Input & Output Clock Toggle Rate” section. Replaced tables 6-73 and 6-74 with Tables 6–75 through 6–83. Input and output clock rates for row, column, and dedicated clock pins are now in separate tables. | |
| February 2006, v2.1 | <ul style="list-style-type: none">● Updated Tables 6–4 and 6–5.● Updated Tables 6–49 through 6–65 (removed column designations for industrial/commercial and removed industrial numbers). | |
| December 2005, v2.0 | Updated timing numbers. | |
| October 2005 v1.1 | <ul style="list-style-type: none">● Updated Table 6–7.● Updated Table 6–38.● Updated 3.3-V PCML information and notes to Tables 6–73 through 6–76.● Minor textual changes throughout the document. | |
| October 2005 v1.0 | Added chapter to the <i>Stratix II GX Device Handbook</i> . | |



Software

Stratix® II GX devices are supported by the Altera® Quartus® II design software, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® II logic analyzer, and device configuration.



Refer to the *Quartus II Development Software Handbook* for more information on the Quartus II software features.

The Quartus II software supports the Windows XP/2000/NT, Sun Solaris 8/9, Linux Red Hat v7.3, Linux Red Hat Enterprise 3, and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink interface.

Device Pin-Outs

Stratix II GX device pin-outs (*Pin-Out Files for Altera Devices*) are available on the Altera web site at www.altera.com.

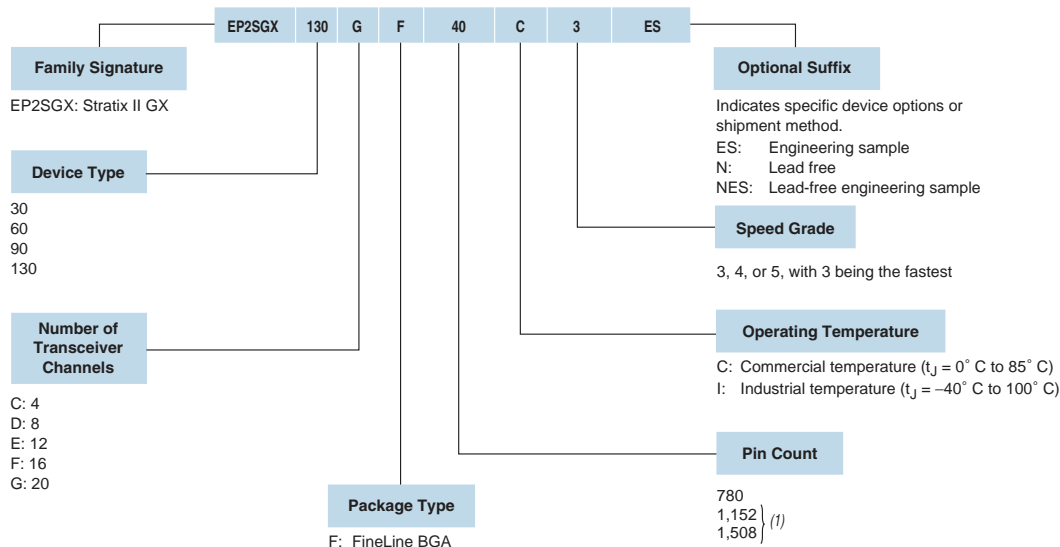
Ordering Information

Figure 5-1 describes the ordering codes for Stratix II GX devices.



For more information on a specific package, refer to the *Package Information for Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*.

Figure 5–1. Stratix II GX Device Packaging Ordering Information



(1) Product code notations for ES silicon for all EP2SGX130 family members (standard and lead free) and EP2SGX90 (lead free) use the following codings to denote pin count: 35 for 1152-pin devices and 40 for 1508-pin devices

Referenced Documents

This chapter references the following documents:

- [Package Information for Stratix II & Stratix II GX Devices](#) chapter in volume 2 of the *Stratix II GX Device Handbook*
- [Pin-Out Files for Altera Devices](#)
- [Quartus II Development Software Handbook](#)

Document Revision History

Table 5–1 shows the revision history for this chapter.

| <i>Table 5–1. Document Revision History (Part 1 of 2)</i> | | |
|---|---|--------------------|
| Date and Document Version | Changes Made | Summary of Changes |
| August 2007 v1.3 | Added the “Referenced Documents” section. | |
| | Minor text edits. | |

Table 5–1. Document Revision History (Part 2 of 2)

| Date and Document Version | Changes Made | Summary of Changes |
|----------------------------------|--|---|
| February 2007 v1.2 | Added the “Document Revision History” section. | Added support information for the Stratix II GX device. |
| June 2006, v1.1 | <ul style="list-style-type: none">● Updated “Device Pin-Outs” section.● Updated Figure 7–1. | |
| October 2005 v1.0 | Added chapter to the <i>Stratix II GX Device Handbook</i> . | |

